

Synthesis and application of titanium nitride for gallium nitride electron devices

Liuan Li

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Department of electrical and electronic engineering

The university of Tokushima

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Chapter 1: Introduction of AlGaN/GaN heterostructure field-effect transistors

§1.1. Background

With the recent upsurge of the wireless communication market, as well as the steady but continuous progress of traditional military applications, microwave transistors are playing critical roles in many aspects of human activities. The requirements for the performance of microwave transistors are becoming more and more demanding. In the personal mobile communication applications, next generation cell phones require wider bandwidth and improved efficiency. The development of satellite communications and TV broadcasting requires amplifiers operating at higher frequencies and higher power to reduce the antenna size of terminal users. The same requirement holds for broadband wireless internet connections as well because of the ever increasing speed or data transmission rate. Because of these needs, there has been significant investment in the development of high performance microwave transistors and amplifiers based on Si, GaAs, SiC and GaN. Figure 1-1 shows the required output power and operating frequency of RF power amplifiers for several military and civil applications. Different materials systems allow us to fulfill different requirements.

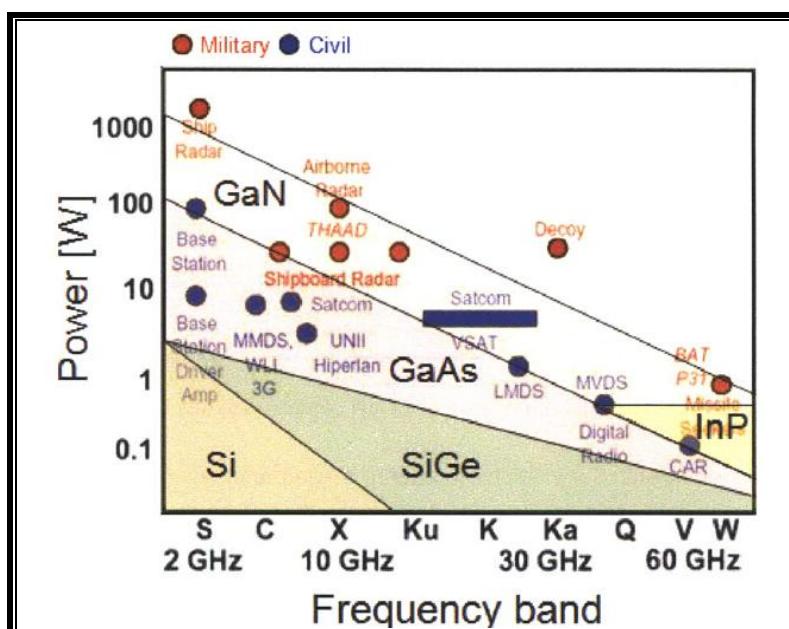


Figure 1-1 required output power and frequency of RF amplifiers.

§1.2. The properties of GaN

Gallium nitride (GaN) based, in particular aluminium gallium nitride (AlGaN)/GaN heterostructure field-effect transistors (HFETs), have become one of the most promising solid-state microwave power devices due to their ability to produce higher power densities at higher frequencies as compared to silicon (Si) and gallium arsenide (GaAs)-based devices. This is attributed to a unique combination of GaN material properties, including wide bandgap (3.4 eV of GaN to 6.2 eV of AlN), large electric breakdown field strengths ($\sim 3 \times 10^6$ V/cm) and high saturation electron drift velocity ($> 2 \times 10^7$ cm/s). These properties are given in Figure 1-2, as well as a wide range of common semiconductor materials for comparison to GaN. The Johnson's figure of merit (JM) calculated from the major parameters are also listed to compare the power-frequency limits of different materials.^[1] The JM gives the power-frequency limit based solely on material properties and can be used to compare different materials for high frequency and high power applications.

	Si	GaAs	4H-SiC	GaN	Diamond
E_g (eV)	1.1	1.42	3.26	3.39	5.45
n_i (cm ⁻³)	1.5×10^{10}	1.5×10^6	8.2×10^9	1.9×10^{10}	1.6×10^{-27}
ϵ_r	11.8	13.1	10	9.0	5.5
μ_n (cm ² /Vs)	1350	8500	700	1200(Bulk) 2000(2DEG)	1900
v_{sat} (10 ⁷ cm/s)	1.0	1.0	2.0	2.5	2.7
E_{br} (MV/cm)	0.3	0.4	3.0	3.3	5.6
Θ (W/cm K)	1.5	0.43	3.3-4.5	1.3	20
$JM = \frac{E_{br}v_{sat}}{2\pi}$	1	2.7	20	27.5	50

Figure 1-2 material properties related to the power performance.

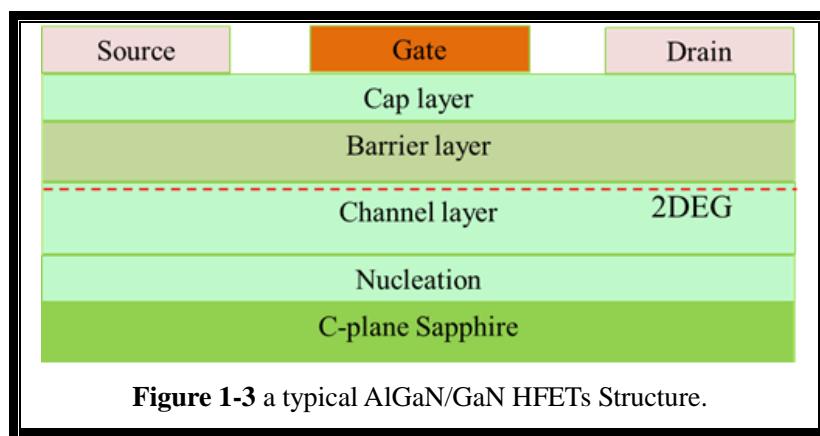
The requirement for high power and high frequency requires transistors based on semiconductor materials with both large breakdown voltage and high electron velocity. From this point of view, wide bandgap materials, like GaN and SiC, with higher JM are preferable. The wide bandgap results in higher breakdown voltages because the ultimate breakdown field is the field required for band-to-band impact ionization. Moreover, both have high electron saturation velocities, which allow high frequency operation. The ability of GaN to form heterojunctions makes it superior compared to SiC, in spite of having similar breakdown fields and saturation electron velocities. GaN can be used to fabricate heterostructure field-effect transistors (HFETs) whereas SiC can only be used to fabricate metal semiconductor field effect transistors.

(MESFETs). The advantages of the HFET include its high carrier concentration and its higher electron mobility due to reduced ionized impurity scattering. The combination of high carrier concentration and high electron mobility results in a high current density and a low channel resistance, which are especially important for high frequency operation and power switching applications.

§1.3. The AlGaN/GaN HFETs Technology

§1.3.1. Typical AlGaN/GaN HFETs Structure

Usually, the GaN-based HFETs are obtained by epitaxial material growth using molecular beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD) methods. The typical epitaxial structure for GaN-based HFETs is shown in Figure 1-3, which is mainly consisted by the following layers (from top to bottom): cap layer, barrier layer, channel layer, nucleation layer and substrate.



Cap layer is usually a thin GaN layer (1-2 nm) that deposited on top of the barrier layer. It can benefit to prevent the oxidation of barrier layer surface, form low resistance Ohmic contact, act as gate insulate and so on. [2,3]

Barrier layer, $\text{Al}_x\text{Ga}_{1-x}\text{N}$ in our case, is the most critical layer in HEMT structure. The bandgap of this material is wider than the channel layer and depends on the aluminium mole fraction x. [4]

Channel or buffer layer, GaN in our case, is a material with the lower bandgap than barrier layer. The semi-insulating (SI) or high resistivity property is to ensure proper drain-source current saturation, complete channel pinch-off, low loss at high frequencies, and low cross-talk between adjacent devices.

Nucleation layer is grown before epitaxing a thicker channel layer to reduce

stress and lattice mismatch to the nonnative substrate. Because the rare of high quality bulk GaN substrate, GaN epitaxy is grown on substrates such as SiC, c-plane sapphire (Al_2O_3) or Si (111). The inserted layer is usually very thin AlN, AlGaN or GaN.

Upon growth of the HFETs structure, three metal electrodes, source (S), gate (G), and drain (D) are made to the top barrier layer by optical lithography and DC reactive sputtering. Both the source and drain terminals are Ohmic contacts while the gate electrode is Schottky. The source is typically grounded while a positive bias is applied to the drain (V_{DS}), controlling the carriers in 2DEG flow from source to drain in the direction parallel to the hetero-interface. While the Schottky gate with a gate-source voltage (V_{GS}) can controls the potential distribution of heterostructure below the contact.

§1.3.2. Spontaneous and Piezoelectric Polarization Effects

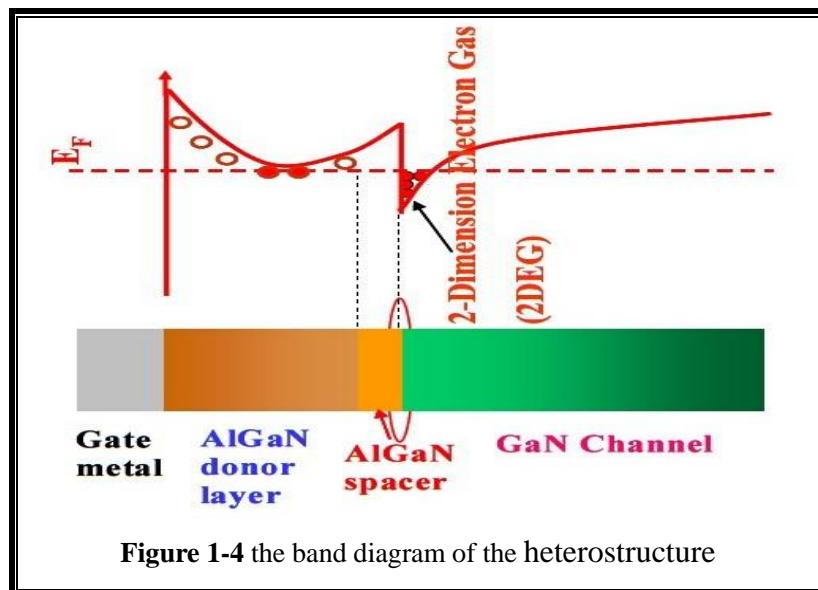
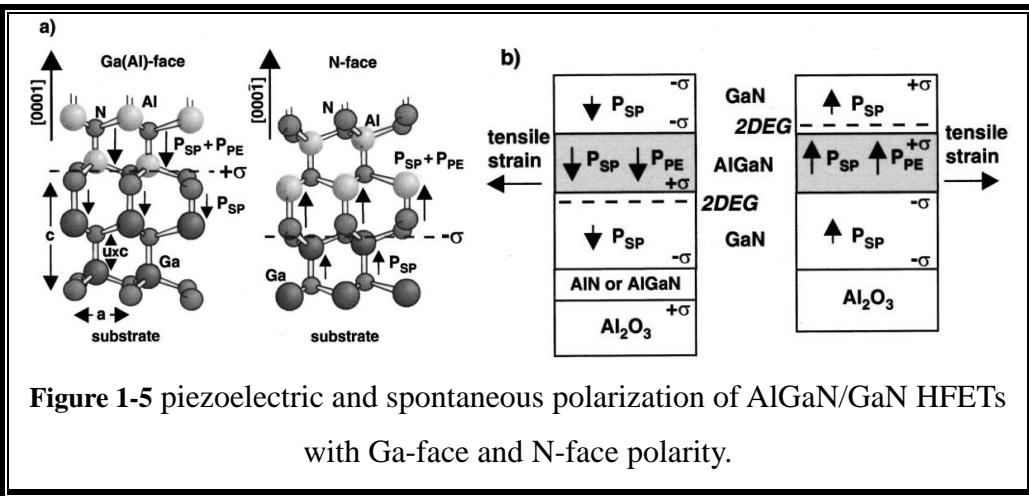


Figure 1-4 the band diagram of the heterostructure

AlGaN/GaN HFET is composed of a thin wide band-gap material (AlGaN as the barrier layer) grown on top of a narrow band-gap material (GaN as the channel layer). The conduction band discontinuity between those two layers will form a triangular quantum well on the GaN-side of the hetero interface (Figure 1-4). When the AlGaN is grown on the GaN, tensile strain builds up at the hetero-interface due to the lattice mismatch. The III-nitride with large piezoelectric coefficient can induce a sizeable piezoelectric polarization (PE) under the presence of this built-in strain. Increasing the

Al-content in the strained AlGaN leads to an increase in piezoelectric polarization.

The crystal structure of GaN is hexagonal or wurtzite. Wurtzite III-nitride crystals can be grown according to two different faces: metallic face: when the top most atoms are metals and nitrogen face: when the top most atoms are nitrogen (Figure 1-5a).[5] The non-centrosymmetric nature of wurtzite crystals induces a sizeable spontaneous polarization (SP) in these crystals without any external field with the polarization vectors are additive along the c-direction. The direction of the spontaneous polarization depends on the face of the crystal (Figure 1-5b). The strength of this spontaneous polarization is in increasing order from GaN to InN, and to AlN.[6]



The discontinuity of spontaneous polarization charge and piezoelectric polarization charge is responsible for the formation of the high concentration 2DEG in the triangular quantum well of AlGaN/GaN HFETs. Since the 2DEG electrons are confined in the triangular quantum well and as a result are spatially separated from the parent ionized impurities, electron mobility will be enhanced in such a structure.

§1.3.3. The operation theory of AlGaN/GaN HFETs

All the different types of HFETs operate in a similar way. The current flowing between the drain and source contacts can be written as follows (rate at which the 2DEG charge moves across the gate):

$$I_D = qn_s V_{eff} W_G, \quad (1-1)$$

where V_{eff} is the effective velocity of the electrons in the channel, n_s is the

2DEG charge density and W_G is the gate width.

The 2DEG carrier density can vary from a maximum value of n_{s0} to a minimum value of zero depending on the gate bias:

$$n_s = \frac{\epsilon_{AlGaN}}{q(d_{AlGaN} + \Delta d)} (V_G - V_T), \quad (1-2)$$

where d_{AlGaN} is the thickness of the AlGaN barrier layer, Δd is the effective distance of the 2DEG from the hetero-interface, and V_G is the gate bias. V_T is the threshold voltage, the gate bias required to pinch-off the channel, which is determined by the composition and doping profile of the AlGaN layer.

As shown in Figure 1-6b, by applying a negative or small gate bias ($V_G \leq V_T$), the channel becomes depleted of carriers, and thus, no current can flow between the drain and source. While with a gate bias of $V_G > V_T$ the device begin to work (Figure 1-6a).

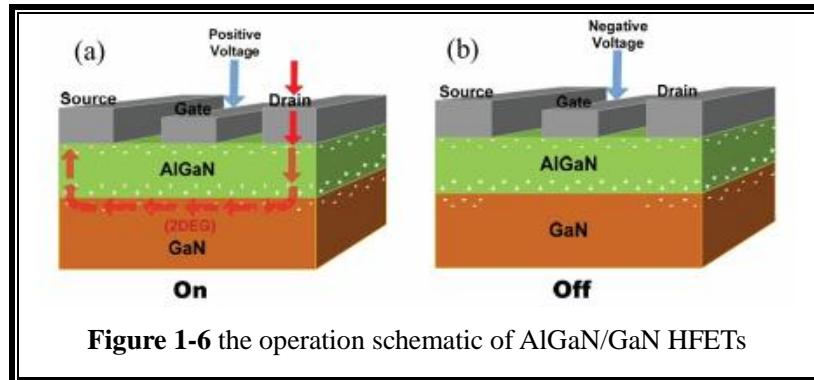


Figure 1-6 the operation schematic of AlGaN/GaN HFETs

When HFETs are biased at low drain voltages ($V_D < V_G - V_T$), the devices are said to be operating in a linear regime, where the electron velocity is linearly related to the electric field strength. However, at high drain biases ($V_D > V_G - V_T$), the effective electron velocity saturates and becomes independent of bias or the electric field strength. Velocity saturation (V_{sat}) occurs due to scattering of electrons with the semiconductor lattice. For practical purposes, devices are

$$I_D = \frac{\epsilon_{AlGaN} W_G V_{sat}}{(d_{AlGaN} + \Delta d)} (V_G - V_T), \quad (1-3)$$

In reality, I_D is not totally independent of V_D . At high values of V_D , high electric fields exist between the drain and gate contacts and may cause electrons to be

injected into the GaN buffer or captured by electron traps. A parallel conduction path may exist between the drain and source contacts. The high drain-to-gate field may also result in an increase in parasitic gate leakage current into the channel. The I_D - V_D curves may also exhibit negative differential resistance at high drain bias voltages, which is characteristic of self-heating effects. These effects cause I_D to be slightly dependent on V_D .

Generally, if the threshold voltage is negative, then the device is called a depletion mode (D-mode) HFETs. When it is positive the device is then called an enhancement mode (E-mode) device. Conventional AlGaN/GaN HFETs are D-mode transistors.

§1.4. Small-signal equivalent circuit of microwave devices

The physical basis of HFETs equivalent circuit is shown in Figure 1-7 and its corresponding small-signal model is shown in Figure 1-8. The intrinsic elements are R_{in} , C_{gs} , C_{gd} , R_{ds} , g_m , τ , and C_{ds} while the extrinsic elements are R_d , R_s , and R_g . In addition, parasitic inductances L_d , L_s , and L_g could be added in series with R_d , R_s , and R_g in the equivalent circuit to account for the effects of device pads. In a HFETs, the conductive channel is controlled by the Schottky barrier gate potential and intrinsic gain is provided by the device transconductance, g_m . The gm is a figure of merit value that measures the effectiveness of the gate in modulating the drain current and is defined in the saturated regime by

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{\epsilon_{AlGaN} W_G V_{sat}}{(d_{AlGaN} + \Delta d)}, \quad (1-4)$$

It is interesting to note that g_m is independent of the gate length (L_G) and gate voltage V_G from the equation. However, in actuality, g_m as well as I_D is dependent on L_G . Velocity overshoot and ballistic effects become important at small L_G and as a result increase V_{sat} . Therefore, higher gm and I_D are obtained for short gate length devices. The actual transconductance is also dependent on V_G . At gate voltages near V_T , the electrons in the 2DEG are pushed away from the heterointerface and thus increase the value of Δd . As V_G is increased away from V_T , Δd decreases and

causes g_m to increase. At large V_G , n_s in the channel saturates, and g_m peaks at this point. A further increase in V_G beyond this point results in carriers residing in the AlGaN layer instead of in the GaN channel. Carriers in the barrier layer suffer a reduced mobility and, as a consequence, reduced velocity. The overall effective velocity of the carriers degrades and causes g_m to decrease with high V_G .

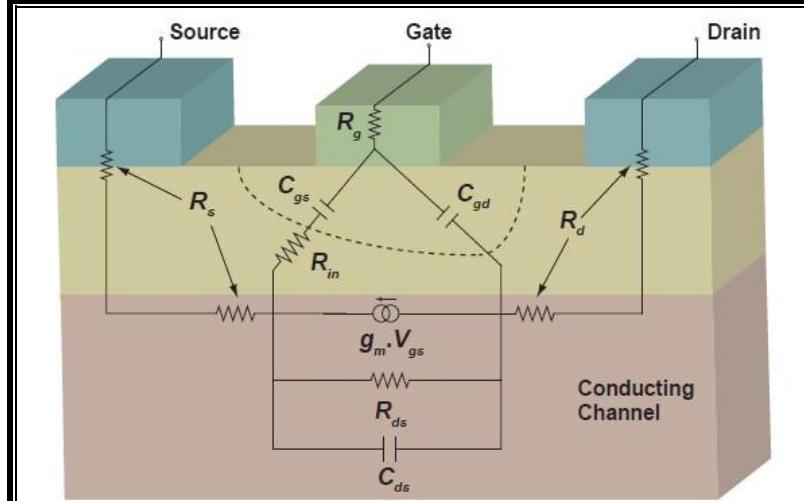


Figure 1-7 physical basis of small-signal equivalent circuit.

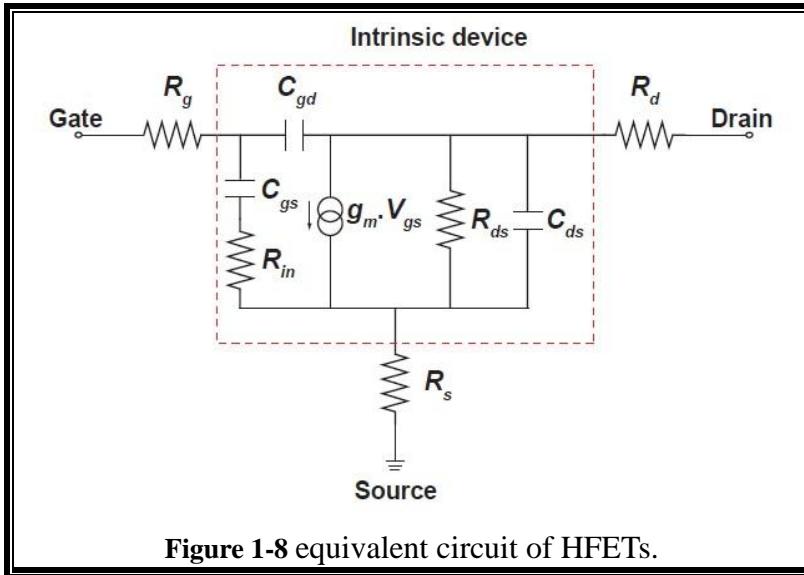


Figure 1-8 equivalent circuit of HFETs.

The g_m as given by Eqn. (1-4) is called intrinsic transconductance ($g_{m,int}$), since the expression does not take into account parasitics such as series source resistance (R_s). The measured transconductance is called extrinsic transconductance ($G_{m,ext}$),

since it includes parasitic effects. The $G_{m,ext}$ is related to $g_{m,int}$ as follows:

$$G_{m,ext} = \frac{g_{m,int}}{(1 + g_{m,int}R_s)}, \quad (1-5)$$

In general, the series source and drain resistances limit the current drive capabilities of FETs. These parasitic resistances lead to lower values of the drain current and higher values of the knee voltage at which the transistor current saturates. Another important parameter in determining the performance of the devices is the transit time (τ) of the electrons. This transit time is related to the unity-current gain cut-off frequency (f_T):

$$f_T = \frac{1}{2\pi\tau_t} = \frac{v_{eff}}{2\pi L_G}, \quad (1-6)$$

The f_T can be derived using a simple small-signal model (Figure 1-8 without access resistances) as:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \quad (1-7)$$

where C_{gs} is the capacitance between gate and source and C_{gd} is the capacitance between gate and drain. The f_{max} can also be derived using a simple small-signal model as:

$$f_{max} = \frac{f_T}{2\sqrt{\frac{R_{in} + R_s + R_g}{R_{ds}} + 2\pi f_T R_g C_{gd}}}, \quad (1-8)$$

where R_{in} is the input resistance and R_g is the metal gate resistance. To maximize f_{max} , the f_T and the resistance ratio $(R_{in} + R_s + R_g)/R_{ds}$ must be optimized in the intrinsic HFETs. The extrinsic resistances R_g and R_s and the feedback capacitance (C_{gd}) have also to be minimized.

§1.5. The motivation of this research

Conventional fabrication processes of the HFETs involve patterning and annealing the source and drain contacts before the formation of the Schottky gate contact because annealing at relatively high temperature is necessary to obtain ohmic contact (Figure 1-9a). After the formation of the ohmic contact, gate electrode is then

patterned and deposited by aligning the ohmic patterns. Due to the alignment process, this approach limits the minimum source-to-gate and drain-to-gate distances and makes it very difficult to obtain small access resistances. Alternatively, a self-aligned-gate (SAG) process is proposed, in which a T-shaped Schottky gate is fabricated and then used as a mask directly for the ohmic metal evaporation (Figure 1-9b). Then, the Schottky gate and the ohmic electrodes are annealed simultaneously to achieve ohmic contacts. This technology is actually a so-called gate-first process. The SAG structure can reduce the source and drain access resistance further by reducing the spacing among the electrodes. The important technologies to form the SAG structure are the formation of T-gate and the Schottky gate structure which can stand the ohmic annealing process. Usually, Ti-based complex multilayer systems such as Ti/Al/Ni/Au, Ti/Al/Ti/Au, Ti/Al/Pd/Au and Ti/Al/Mo/Au are widely used to form ohmic contacts on n-type GaN and AlGaN/GaN HFETs. However, to form the ohmic contact with Ti-based multilayers on GaN-based materials, the formation of a metallic compound and nitrogen vacancies are needed, which show great dependence on the annealing temperature (commonly above 700°C). Therefore, an appropriate gate stack that can stand such a high ohmic annealing temperatures is necessary for fabricating SAG devices. However, the recent Ni or Cu gate materials on AlGaN/GaN HFETs could not stand the ohmic annealing temperature.

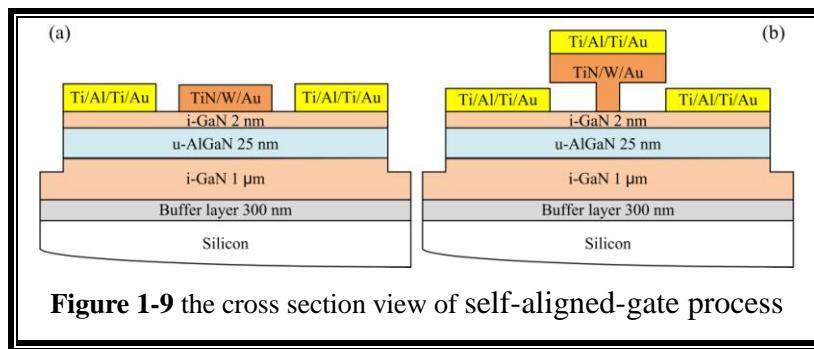


Figure 1-9 the cross section view of self-aligned-gate process

§1.6. Outline of Thesis

This thesis reports on the deposition and evaluation of TiN for the application in GaN based devices. This thesis is divided into four sections:

Chapter 2 elucidates the evaluation of the thermal stability of different refractory metal nitrides used as Schottky electrodes on GaN. After evaluating the thermal stability and the current-voltage performance, we regard TiN as the proper material

for a Schottky electrode. We then produce TiN films using different N₂/Ar reactive/inert sputtering gas flow ratios. Measurements of the variation of the growth rate and the resistivity of the films versus the sputtering gas composition are obtained. The thermal stability of the different films is also investigated by prolonging the treatment time at 800 °C. The mechanism of variation in the gate resistivity is also analyzed.

Chapter 3 establishes the GaN Schottky barrier diodes (SBDs) with low turn-on voltage developed for microwave rectification. The diodes with reactively sputtered TiN electrodes have a lower turn-on voltage compared with the diodes with Ni electrode, while the on-resistance, the reverse leakage current and the reverse breakdown characteristics are comparable to each other. Theoretically, the SBDs with TiN electrodes can enhance the efficiency of a rectenna circuit at 2.45 GHz from 84% to 89% when the turn-on voltage decreases from 1.0 to 0.5 V.

In Chapter 4, we evaluated the annealing temperature and time dependent electrical properties of AlGaN/GaN heterostructure field-effect transistors utilizing TiN/W/Au as the gate electrode. By changing the annealing temperature, the ohmic contact was minimum at 800 °C and the devices showed the lowest on-resistance and highest maximum drain current. By prolonging the annealing from 0.5 to 10 min at 800 °C, good device performance was achieved when the annealing time was 1 and 3 min, while the device performance degraded with increasing annealing time. These results demonstrated that the TiN/W/Au gate is suitable for application in the self-aligned-gate process for AlGaN/GaN HFETs.

In Chapter 5, we focus on the fabrication of metal-oxide-semiconductor hetero-structure field effect transistors to further improve the performance of devices. the influence of deposition conditions and post annealing upon the device performance of the sputtering deposited Al₂O₃ and HfON is reported. The metal-oxide-semiconductor heterostructure field-effect transistors with small hysteresis and low leakage current were obtained by inserting Al₂O₃ and HfON dielectric deposited with a medium O₂/Ar ratio and post-annealing.

The dissertation is concluded by reporting on the future work required to improve the properties of the devices in Chapter 6.

Chapter 2: Synthesis and characterization of TiN

§2.1. The selection of gate material for self-aligned-gate process

The AlGaN/GaN heterostructure-based heterostructure field-effect transistors (HFETs) are excellent candidates for high-power and high-frequency electronic devices.[7,8] To achieve a high-temperature performance, it is very desirable to produce gate contacts with a large Schottky barrier height (SBH) and excellent thermal stability. In high-frequency applications, it is beneficial to minimize the source-to-gate and drain-to-gate distances for smaller access resistances using a self-aligned-gate (SAG) process. In this process, a T-shaped Schottky gate is fabricated and used directly as a mask for ohmic metal evaporation. The Schottky gate and the ohmic electrodes are then annealed simultaneously to obtain ohmic contacts. The optimized annealing temperature of the ohmic contact in our process is 800-850°C with an annealing time of 1 min. Therefore, the Schottky contact must be able to withstand this high temperature during the source-drain ohmic contact annealing process.[9,10] For this purpose, refractory metal nitrides such as WN, TiN, TaN, MoN, and MoSiN etc., which possess a suitable work function, low resistivity and good thermal stability, are possible candidates. [11-13]

In previous studies, we evaluated the electrical performance of Schottky contacts produced using different kinds of refractory metal nitrides such as TiN, MoN, TaN, MoSiN, WTiN, ZrN, and HfN, on GaN ($1 \times 10^{17} \text{ cm}^{-3}$) using reactive sputtering in an ambient Ar and N₂ mixture sputtering gas.[14] Rectification characteristics were obtained and the estimated Schottky barrier heights (SBHs) of most of the contacts increased after the introduction of N₂ in the sputtering gas, which suggests their potential as Schottky metals on GaN. However, the reverse leakage current of the WN and WSiN contacts was about two orders of magnitude larger than that of the other samples. The results also demonstrated that the resistivity of TaN, ZrN, and HfN were relatively larger than that of the other samples, and the adhesion of WTiN on GaN was deficient. This left TiN, MoN, and MoSiN as good candidates for Schottky contact metals on GaN because they could be obtained easily by reactive sputtering with nitrogen as the reactive gas, and they showed a relatively smaller resistivity, good adhesion and less leakage current on the GaN Schottky contact. The TiN-gated AlGaN/GaN HFETs have been fabricated for thermal stability evaluation.[15] It was

found that the devices still presented good pinch-off characteristics and a low gate leakage current even after annealing for 5 min at 850°C. However, the drain current showed obvious degradation when the thermal treatment period was prolonged owing to the increased gate resistance, which was nearly doubled after annealing for 10 min and was tripled after 30 min. A stack structure created by depositing a W/Au (30/70 nm) cap layer above the TiN was found to efficiently alleviate the gate resistance increase, with only a slight increase observed after annealing for 10 min at 800°C.[16] However, the mechanism behind the increasing TiN gate resistance is not apparent, and further improvement of the electrode performance will also be valuable.

With the reactive sputtering method, the structural, electrical and optical properties of the metal nitrides usually depend upon the nitrogen content in the reactive/inert sputtering gas mixture. Earlier work suggests that a gradual increase in the nitrogen content can change the lattice constant and preferred orientation (or texture).[17] Furthermore, variation in the resistivity showed a relationship with the nitride composition.[18] In this study, we first synthesize the three kinds of nitrides mentioned above using DC magnetron reactive sputtering. To evaluate their thermal stability, the samples are annealed at 850°C for 1 min to parallel the annealing of Schottky contacts at 800-850°C in the SAG process. After evaluating the thermal stability and the current-voltage performance, we regard TiN as the proper material for a Schottky electrode. We then produce TiN films using different N₂/Ar reactive/inert sputtering gas flow ratios. Measurements of the variation of the growth rate and the resistivity of the films versus the sputtering gas composition are obtained. The thermal stability of the different films is also investigated by prolonging the treatment time at 800 °C. The fluctuation in the gate resistivity is analyzed using x-ray diffraction (XRD), Raman spectroscopy and x-ray photoelectron spectroscopy (XPS) results.

§2.2. The synthesis of titanium nitride

The commercial n-GaN wafers used in this experiment were grown on (0001) sapphire substrate by metal organic chemical vapor deposition (MOCVD). The vertical structure of the wafer from bottom to top consists of a buffer layer (about 30 nm thick), a Si-doped ($5 \times 10^{18} \text{ cm}^{-3}$ dopant density, 1 μm thick) GaN layer, and a Si-doped ($1 \times 10^{17} \text{ cm}^{-3}$ dopant density, 1 μm thick) Schottky contact layer. To

maintain a uniform current flow between the ohmic contact and the Schottky contact, a circular Schottky pattern with a diameter of 160 μm was adopted. The ohmic contact was placed on the same side as the Schottky contact with a separating distance of 15 μm to simplify the process.

A standard lift-off technology was used to form both the ohmic and the Schottky contacts. Ohmic contact was formed using a Ti/Al/Ti/Au (50/200/40/40 nm) multi-layer structure, a fixed structure which is being adopted in our process system. By evaluating the ohmic contact performance under different annealing temperatures and in an N_2 ambient environment, a resistance of 0.66 $\Omega \text{ mm}$ was obtained at 800 $^{\circ}\text{C}$ for 1 min. Prior to the metal nitride deposition process, the sample surfaces were cleaned by O_2 plasma ashing and immersion in a diluted HCl (HCl:H₂O=1:1) solution for 5 min to remove any oxide layer that developed after the lithography process. The metal nitride films were deposited using reactive sputtering in an Ar and N_2 mixture ambient environment with Ti, Mo, and MoSi targets. The background vacuum was kept at 2×10^{-5} Pa. Before reactive sputtering, the target was cleaned by sputtering for 10 min in an Ar ambient environment with a power of 150 W. The sputtering power was fixed at 75 W and the N_2/Ar ratio was 3:15 sccm with a chamber pressure of 0.14 Pa during reactive sputtering. Pre-sputtering for 10 min was also conducted under the same conditions as the process sputtering. To study the effects of thermal treatment on the Schottky contacts, samples with the three different metal nitrides were annealed at 850 $^{\circ}\text{C}$ for 1 min (N_2 ambient) in rapid thermal annealing (RTA) equipment. For the TiN gate films deposited with different N_2/Ar ratios, the thermal treatment was carried out at 800 $^{\circ}\text{C}$ for 1, 3, and 5 min.

§2.3. The Schottky contact of TiN on n-GaN

The experimental current–voltage (*I-V*) data of Schottky contact was analyzed by the well-known thermionic emission TE theory. At forward-bias, the TE theory predicts that the *I-V* characteristic is given as follows: [19]

$$I = A_e A^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right], \quad (2-1)$$

Where A_e is the effective diode area, A^* is the effective Richardson constant of 26.8 $\text{Acm}^{-2}\text{K}^{-2}$ for n-type GaN, T is the absolute temperature, q is the electron charge, V is the forward-bias voltage, k is the Boltzmann constant, Φ_b is the experimental

zero-bias apparent barrier height and n is the ideality factor.

When $qV \geq 3kT$, $\exp\left(\frac{qV}{nkT}\right) \geq 1$, the equation can be simplified as

$$I = A_e A^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \exp\left(\frac{qV}{nkT}\right) \text{ or } J = A^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \exp\left(\frac{qV}{nkT}\right), \quad (2-2)$$

$$\text{Then, } \ln J = \frac{qV}{nkT} + \ln(A^* T^2) - \frac{q\phi_b}{kT} \quad (2-3)$$

The experimental values of the barrier height and the ideality factor for the device were determined from intercepts and slopes of the forward-bias $\ln I$ versus V plots as shown in Figure 2-1, respectively.

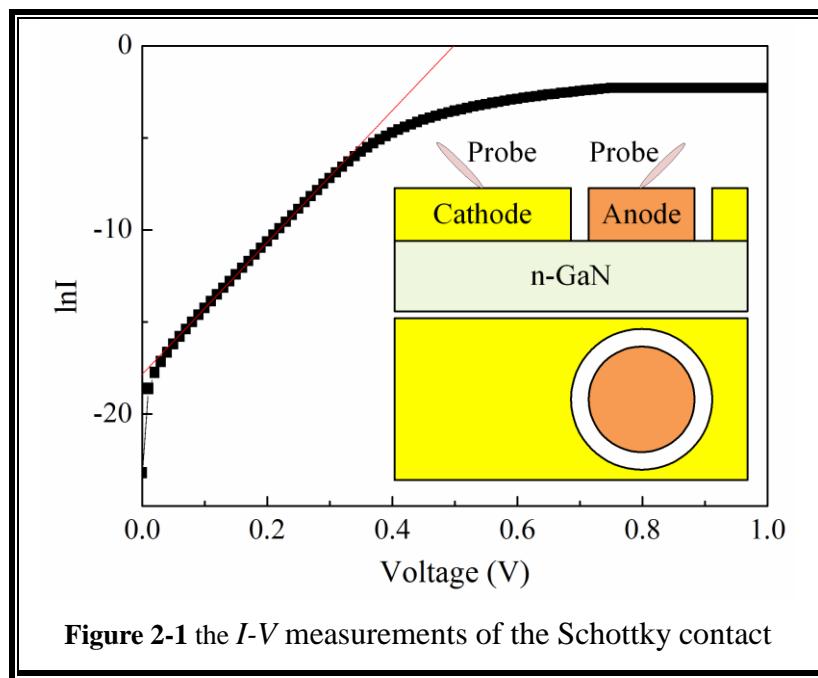


Figure 2-1 the I - V measurements of the Schottky contact

The I - V characteristics of the TiN, MoN, and MoSiN Schottky contacts on n-GaN before and after 850°C annealing for 1 min are shown in Figure 2-2. All as-deposited samples show good rectifying characteristics with a relatively small reverse leakage current. The forward bias curves can be fitted into two linear regions where the lower bias region is determined by the generation-recombination effect and the intermediate region is attributed to thermionic emission. The upper part of the curve shows curvature owing to the contribution of the series resistance of the device. These curves demonstrate that the TiN and MoN electrodes still exhibit rectifying characteristics after thermal treatment, even though the reverse leakage current increases somewhat. However, the MoSiN contact degrades to an ohmic-like contact

(inset of Figure 2-2) with a large reverse leakage current. The mechanism responsible for this degradation is considered to be the presence of Si without nitridation in the MoSiN film. Silicon acts as a donor in the GaN and may diffuse into the GaN layer, which would create an n^+ -GaN layer on the surface.[20] If this occurs, the leakage current of the Schottky contact will increase due to tunnel transport, and the contact will become ohmic-like. The thermal treatment creates an obvious effect, causing an increasing reverse leakage in MoN and an increasing gate resistance in TiN.

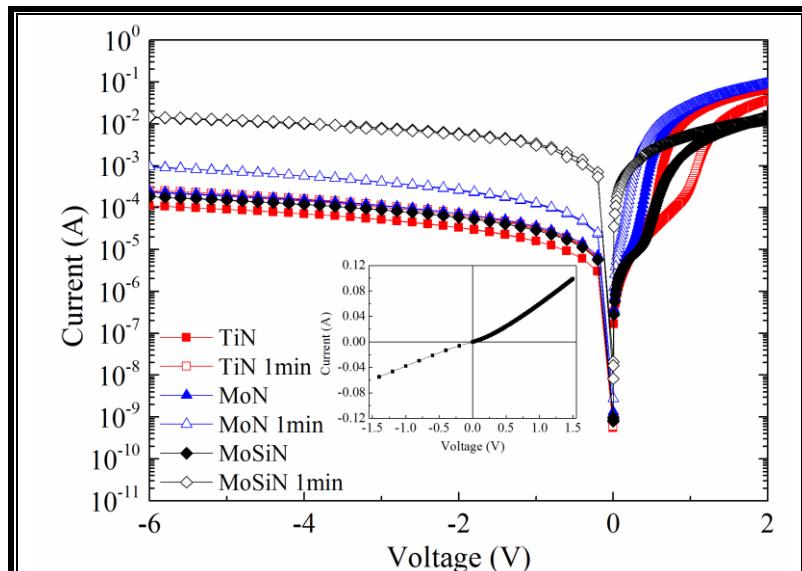


Figure 2-2 the current-voltage curves of different Schottky contacts on GaN before and after thermal treatment.

The experimental values of the Schottky barrier height (SBH) and the ideality factor, n , of the device are deduced from the intercepts and slopes of the linear regions present in the natural log of the forward-bias current ($\ln I$) versus voltage (V) plots using the thermionic emission theory. The TiN device has the highest SBH of 0.56 eV, while the SBH is only 0.35 eV for MoN. However, the ideality factors for all samples are 1.5~1.9, which suggests that in addition to thermionic emission, other carrier transport mechanisms may exist for these diodes, such as defect-assisted tunneling. When considering the thermal stability and SBH of these devices, we regard TiN as the proper material for the Schottky electrode and, therefore, we further investigate the electrical properties of TiN on GaN under different sputtering conditions.

To evaluate the effect of the precursor composition, we deposit TiN films on GaN using different N_2/Ar reactive/inert sputtering gas ratios (nitrogen percentage) of

0:18 (0%), 1:17 (5%), 3:15 (15%), 7:11 (40%), 11:7 (60%), and 15:3 (85%) sccm. The I-V characteristic of the sample with a pure Ti contact shows an ohmic-like contact with a reverse leakage current very similar to the forward current (inset of Figure 2-3). The I-V curves of the other TiN contact samples are all comparable to each other, showing good rectification characteristics and a reverse leakage current of $\sim 10^{-5}$ A (Figure 2-3). The sample with an N₂/Ar ratio of 11:7 (60% N₂ sputtering gas content) exhibits the lowest reverse leakage current and the best forward characteristics.

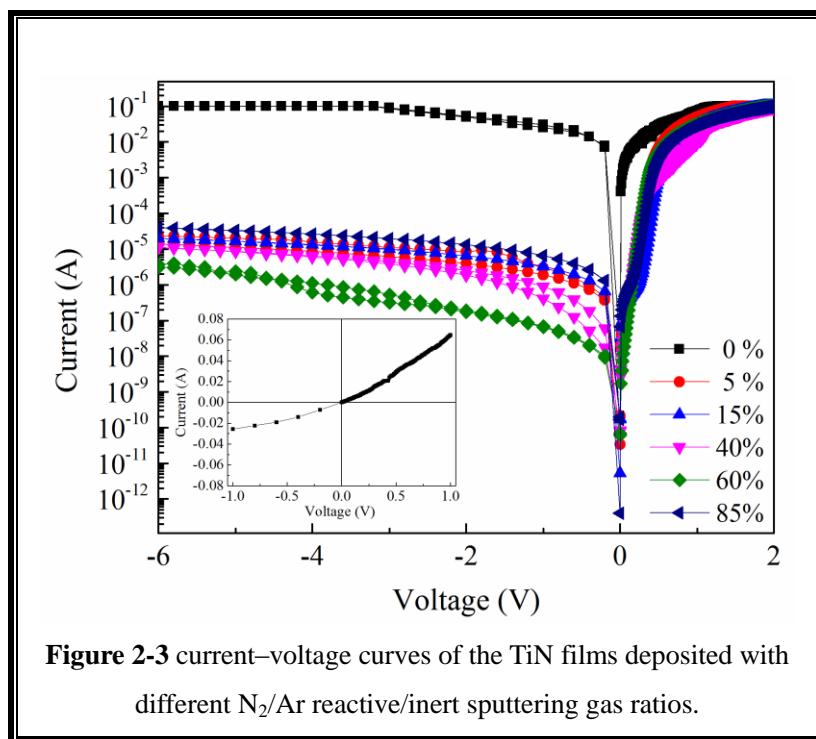


Figure 2-3 current–voltage curves of the TiN films deposited with different N₂/Ar reactive/inert sputtering gas ratios.

The average SBH calculated from the thermionic emission theory for the samples created with different N₂/Ar sputtering gas ratios is 0.5 eV, with SBH values that are comparable for all samples and ideality factors that range from 1.05~1.4 (Figure 2-4). As shown by the I-V characteristics, the sample grown with an N₂/Ar reactive/inert sputtering gas ratio of 11:7 (60% N₂ sputtering gas content) has the lowest ideality factor of 1.05, which is owing to the intimate contact with the semiconductor. The metal work function can be affected by the texture of the TiN and by localized crystalline orientation variation at the TiN interface.[21] The typical XRD spectra of the samples on sapphire, after normalization using the (111) peak, shows four peaks at 33.9 °, 35.9 °, 71.4 °, and 76.4 °(Figure 2-5). The peaks appear as pairs corresponding to the radiation of Cu-K_α (right peak) and Cu-K_β (left peak). The

first and second peak pairs correspond to the TiN diffraction patterns from the (111) and (222) planes, respectively, implying that the crystalline quality and orientation are similar for all samples deposited with varying nitrogen sputtering gas content. Furthermore, the actual nitrogen content of the samples, as determined by quantifying the Ti-2p and N-1s peaks from the XPS data, is 80.49%, 84.50%, 87.20%, 85.62%, and 82.06% for the samples with nitrogen deposition gas percentages of 5%, 15%, 40%, 60%, and 85%, respectively. These results show that all of the TiN films are Ti-rich with similar actual nitrogen contents, excepting that the sample grown with 5% N₂ sputtering gas content has a slightly lower actual nitrogen content than the rest. Examination of the XRD and XPS results implies that the possession of a similar film structure and composition causes the work function of the TiN to be essentially independent of the N₂/Ar sputtering gas ratio.

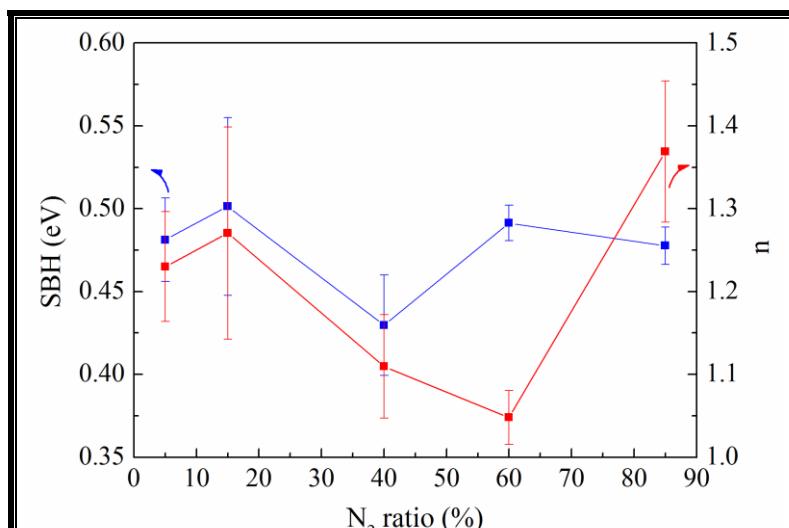


Figure 2-4 the Schottky barrier heights and ideality factors of the TiN films deposited with different N₂/Ar gas ratios.

§2.4. The resistivity variation of TiN upon annealing

The average sputtering rates were calculated by dividing the total film thickness with the respective deposition times. Figure 2-6 shows the sputtering rates versus the N₂/Ar ratios to present the effect of precursor composition. It was about 1.7 nm/min in pure Ar ambient and decreased to about 0.38 nm/min with adding 40% nitrogen, then slightly increased to 0.45 nm/min at higher nitrogen content. Generally, the sputtering rate is determined by the Ar atoms that possess relative heavier mass.

Therefore, when increase the nitrogen concentration, the decrease of sputtering yield as well as the nitride of the surface of the Ti target will cause the decrease of deposition rate.[22]

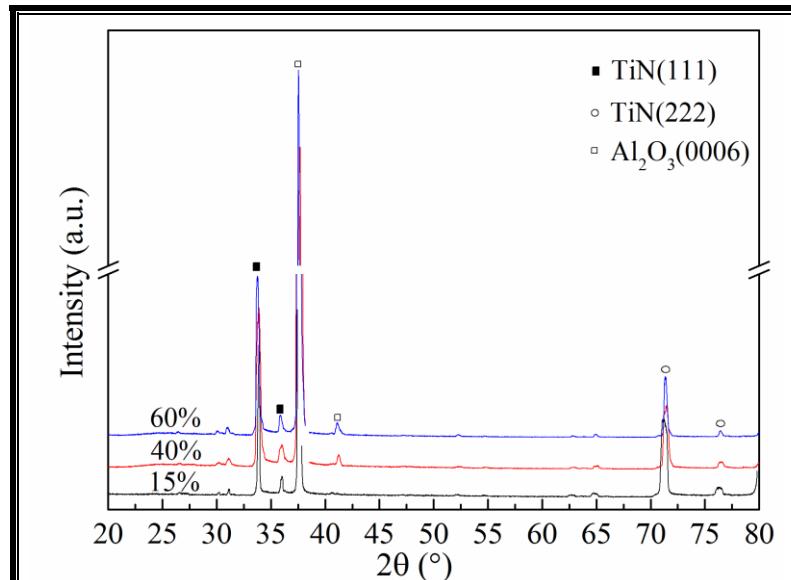


Figure 2-5 typical XRD spectra of the TiN films deposited with different N₂/Ar reactive/inert sputtering gas ratios.

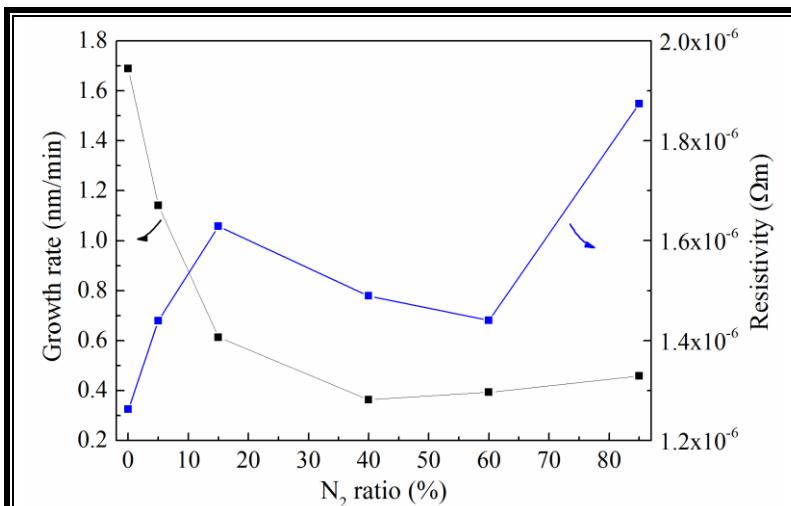


Figure 2-6 the growth rate and resistivity of the TiN films deposited with different N₂/Ar gas ratios.

The four-probe method using a bridge structure as shown in Figure 2-7a is used to determine the sheet resistance of metal nitride films deposited on insulator/semi-insulator substrates, where a constant current is supplied by two probes and a second set of probes are used to measure the voltage drop. The total resistance is

given by

$$R = \frac{V_{23}}{I_{14}} = \rho_s \frac{L}{W} \quad (2-4)$$

where $V_{23} = V_2 - V_3$, I_{14} is the current flowing from contact 1 to contact 4, ρ_s the sheet resistance, L the length, W the width. Usually, the length is about $400\mu\text{m}$ while W is only some μm . To minimize the stander error, we designed a series of width ($W = 3, 6, 9, 12$ and $15\mu\text{m}$), then

$$R = \rho_s \frac{L}{W + \Delta W}, \frac{1}{R} = \frac{1}{\rho_s L} (W + \Delta W) = \frac{W}{\rho_s L} + \frac{\Delta W}{\rho_s L} \quad (2-5)$$

From the slope of the $\frac{1}{R} \propto W$ plotting (Figure 2-7b), we can deduce the ρ_s and the buck resistance by multiply the ρ_s with the thickness of the film t.

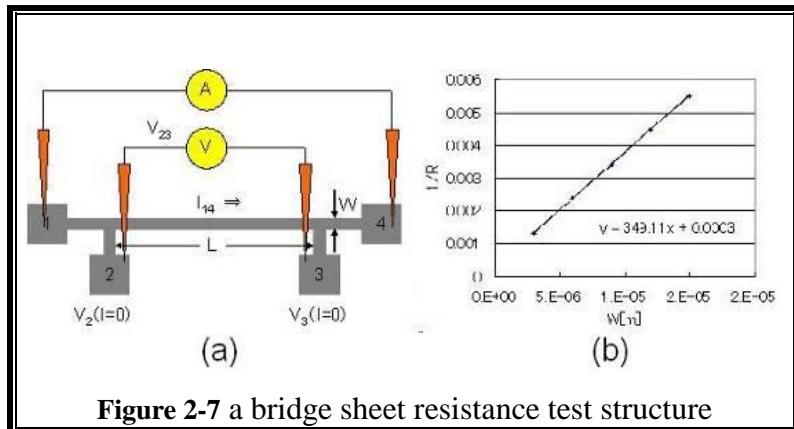
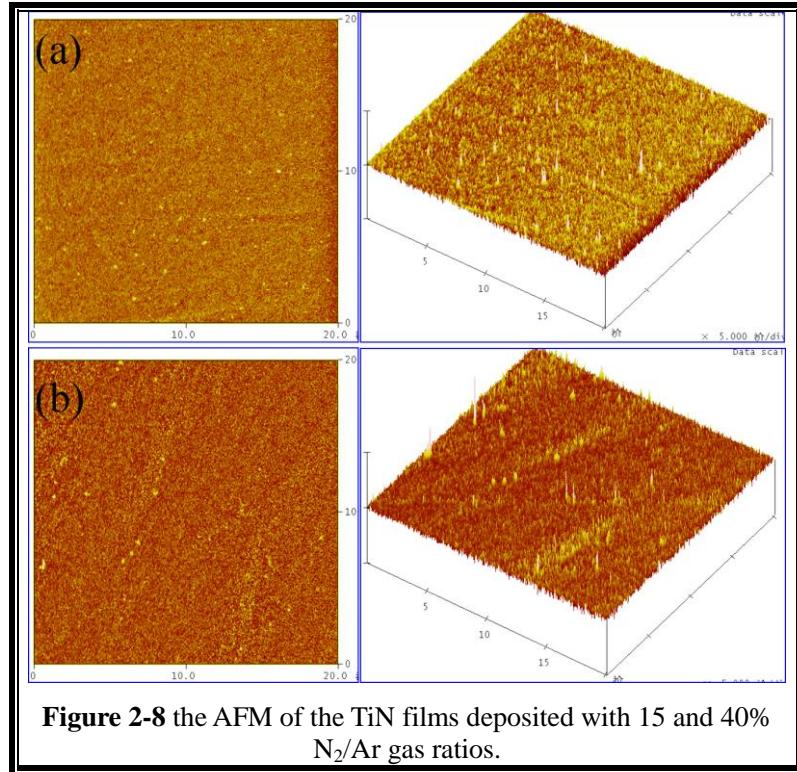


Figure 2-7 a bridge sheet resistance test structure

The resistivities of the films deposited on sapphire were measured using a four-probe method and were plotted versus the nitrogen proportion (Figure 2-6). For the formation of TiN by reactive sputtering method, it has been supposed that a gradual increase of nitrogen contents in metal films led to transition to nitride films. [23] In our case, the resistance of the obtained film increased form $1.3 \times 10^{-6} \Omega \text{ m}$ in pure Ar ambient to about $1.6 \times 10^{-6} \Omega \text{ m}$ for the sample with 15% nitrogen. Then, it showed slight decrease with medium nitrogen content (40%, and 60%). Finally, it increased to about $1.86 \times 10^{-6} \Omega \text{ m}$ with 85% nitrogen. We have carried out XRD (Figure 2-5) and AFM (Figure 2-8) measurements to find some hints of the discrepancy. However, those two group samples show similar crystalline and surface morphologies. Basically, the resistivity of a film depends on the Ti content and the film density. A relative lower growth rate can obtain higher film density, and then

lower resistivity. A sample with higher Ti content will become conductive. In the region of medium nitrogen content, we got lowest growth rate and similar nitrogen content, and hence the lowest resistivity.



The variation of the film resistivity versus thermal treatment time (at 800 °C) presented obvious sputtering condition dependence (Figure 2-9). When annealed for 1 min, the resistance showed decrease which may be due to the increase on film density. After annealing, some voids in the film may disappear owing to the diffusion within the film. After that, the resistance increased almost linearly versus annealing time. Evidently, the samples deposited with different sputtering condition can be divided into two groups by the incremental of resistivity. The resistivity of the films deposited with related lower or higher nitrogen percentage showed drastic increasing after annealing for 5 min, while the increase on the resistivity of the films deposited with medium nitrogen percentage was not so obvious. Besides of the similar structure and composition, Raman and XPS investigation, which will be described in the following sections, demonstrate that the oxidation and/or nitridation occurs mainly on the surface of all the samples with no obvious discrepancy between each other. At a medium N₂ percentage, the relative lower growth rate causes high density preventing

the film from oxidation and/or nitridation. The films with higher density may show a better thermal stability.

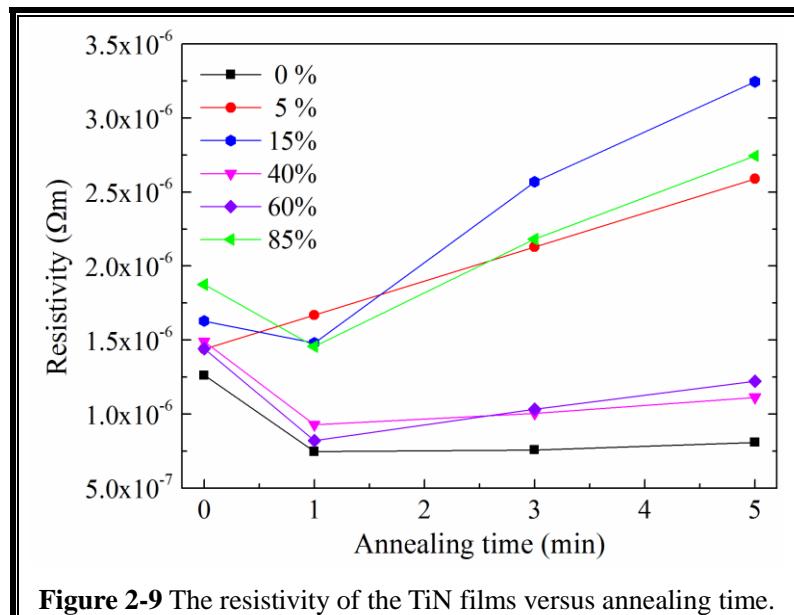


Figure 2-9 The resistivity of the TiN films versus annealing time.

§2.5. The mechanism of resistivity variation

Raman spectra excited by the 538-nm laser light were used to analyze the effect of RTA process. Before annealing (Figure 2-10), no obvious peak was detected for the sample deposited with pure Ar while spectra of other samples were dominated by the peaks at about 200, 310 and 550 cm⁻¹, which can be attributed to first-order transverse acoustic (TA), longitudinal acoustic (LA) and optical (O) mode, respectively. The appearance of the broad and weak peak centered at approximately 1110 cm⁻¹ was owing to the second-order optical (2O) mode.[24] The presence of point defects (Ti, N vacancies) destroys the inversion symmetry, thus allowing first-order Raman scattering, which is forbidden in perfect stoichiometric NaCl structure compounds. It was found that the intensities of all peaks decreased and the first-order line showed slightly shift toward lower frequency when increased the nitrogen portion in source gas, implying the decrease of N vacancy concentration.[25] This may be attributed to the lower growth rate at a higher nitrogen portion, resulting in a better bonding status between N and Ti atoms. The RTA process affects the Raman spectra obviously as shown in Figure 2-11. Characteristic TiN first-order peaks can be detected from the sample deposited with pure Ar after annealed for 5 min, implying the nitride of Ti. For other samples, the Raman peaks became more

intense and sharper. Additionally, three peaks centered at about 830, 1350 and 1600 cm^{-1} became visible which is attributed to the oxidation of films as discussed later.

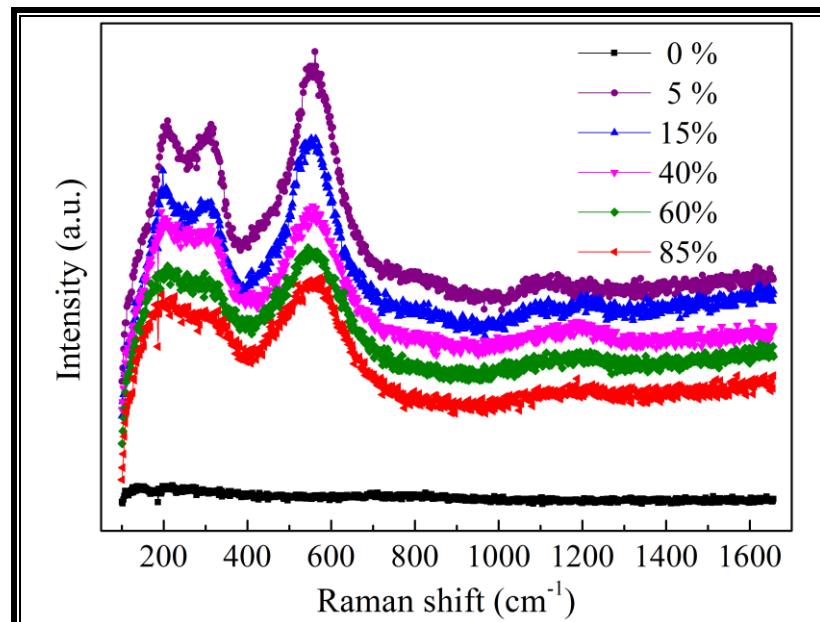


Figure 2-10 Raman spectra of un-annealed TiN films deposited with different N_2/Ar reactive/inert sputtering gas ratios.

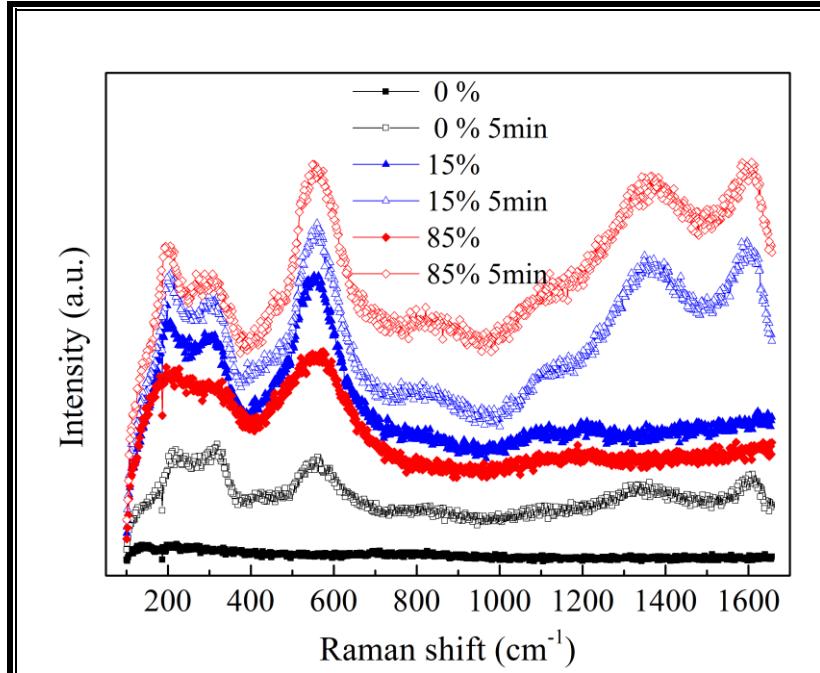


Figure 2-11 effect of annealing on the Raman spectra of TiN films.

The effect of anneal on the films also evaluated by XPS. Figure 2-12 is a typical normalized spectra of un-annealed TiN deposited with N_2 percentage of 15%.

The spectra detected on the surface show obvious discrepancy as compared with that after sputtered for 2 and 4 min. On the film surface, the Ti-2p spectrum can be fitted with four peaks which can be attributed to amorphous TiO_2 (Ti-2p^{3/2}: 458.6 eV, Ti-2p^{1/2}: 464.5 eV), intermediate phase (Ti-2p^{3/2}: 456.7 eV), and TiN (Ti-2p^{1/2}: 461.9 eV), respectively.[26] The spectra of sample after sputtered mainly consisted by TiN (Ti-2p^{3/2} 454.4 eV, Ti-2p^{1/2}: 460.3 eV), intermediate phase (Ti-2p^{3/2}: 456.3 eV), and TiO_2 (Ti-2p^{1/2}: 463.1 eV). The major peak in the corresponding N-1s chemical binding state is centered at about 396.5 eV with shoulder at around 399 eV. The peak at about 396.5 eV was assigned to titanium nitride while the peak located at around 399 eV is assigned to existence of N-O, N-C, and N-N bindings which are molecularly chemisorbed on the surface of the films.[27] After sputtered, the intensity of peak at about 396.5 eV increased obviously and dominated the curve. In the O-1s core level spectra, the major peaks appear around 530 eV, which can be assigned to the lattice oxygen of TiO_2 ,[28] with a clearly visible broadening peak on the higher binding energy side of 531.6 eV. There are two kinds of opinions in explaining the peak at 531.6 eV. One attributes it to the presence of adsorbed oxygen.[29] The other thinks the appearance of this additional peak is the formation of titanium oxynitride.[30] Combining the XPS spectra of N-1s and Ti-2p, we think that the additional peak at 531.6 eV is mainly owing to titanium oxynitride. Base on those spectra, the oxidation of TiN is mainly occurred in the surface layer.

M. Wittmer et. al. and I. Suni et. al. have investigated the oxidation of TiN in the oxygen ambient environment.[31,32] The results demonstrate that prolonged oxidation of TiN leads to increasing thicknesses of the TiO_2 layer. However, the dependence upon the time is not in linear but follows a parabolic law, namely the oxide thickness as a function of the square root of the oxidation time. This means that the oxidation of TiN is diffusion limited, indicating that the diffusion of oxygen through the already grown TiO_2 is the rate limiting process. Thus the thickness d of the TiO_2 is given by $d = 2\sqrt{Dt}$, where D is the diffusion coefficient of the oxygen diffusion in TiO_2 , and t is the oxidation time.

It was found that annealing for 5min mainly affected the phase composition in the surface layer (Figure 2-13), namely, the intensity of amorphous TiO_2 and intermediate phase in the Ti-2p as well as the N-1s peak increasing. This phenomenon

can be attributed to the oxidation and/or nitridation of TiN, resulting in the increase of resistivity.

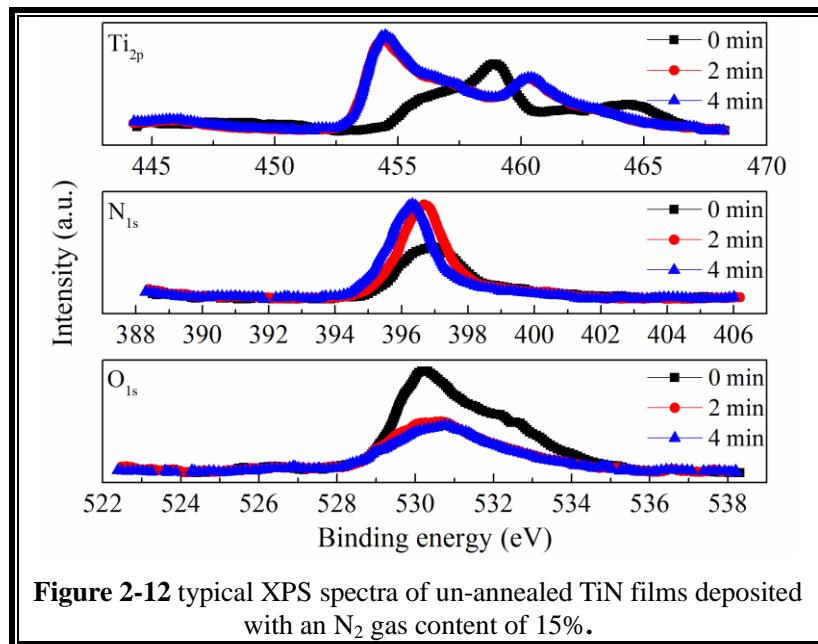


Figure 2-12 typical XPS spectra of un-annealed TiN films deposited with an N_2 gas content of 15%.

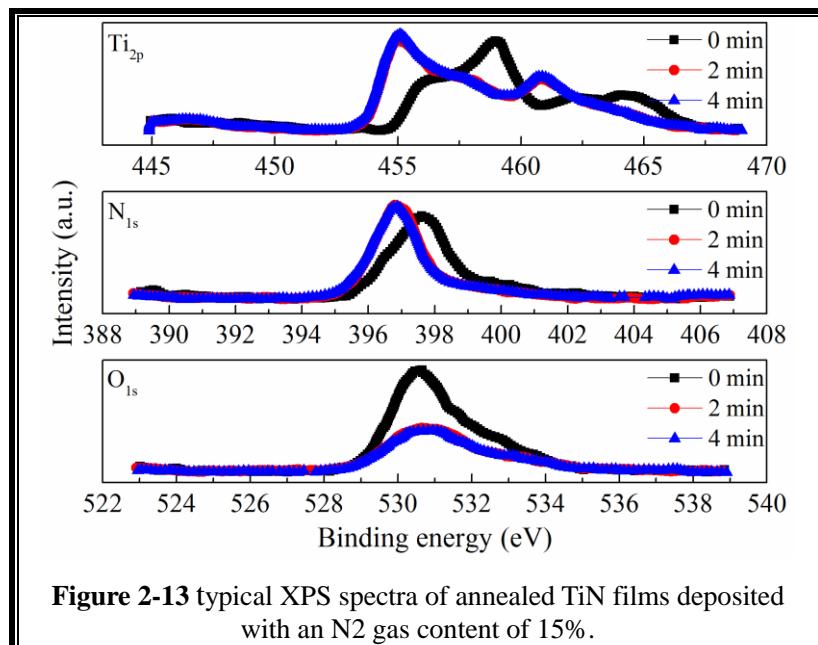


Figure 2-13 typical XPS spectra of annealed TiN films deposited with an N_2 gas content of 15%.

Usually, the TiN exhibits a gold-like color, which results from the high reflectance of the TiN films at the red end of the visible spectrum and the low reflectance near the ultraviolet region. [33] Figure 2-14 is the optical photo of samples deposited with a N_2 ratio of 40% before (a) and after (b) annealed at 800 for 5min. Obviously, the surface color of the sample changed from golden-brown to

bright-golden, which is due to a variation on the reflective index, suggesting a modification on the film structure and/or composition. [34] As presented in chapter 3, a W/Au cap layer can alleviate the increment of film resistance. This is consist with the previous report that the interfacial reaction should not present any kinetic limitation to oxidation when the metal coating film is present, and the overall oxidation rate is greatly reduced. [35]

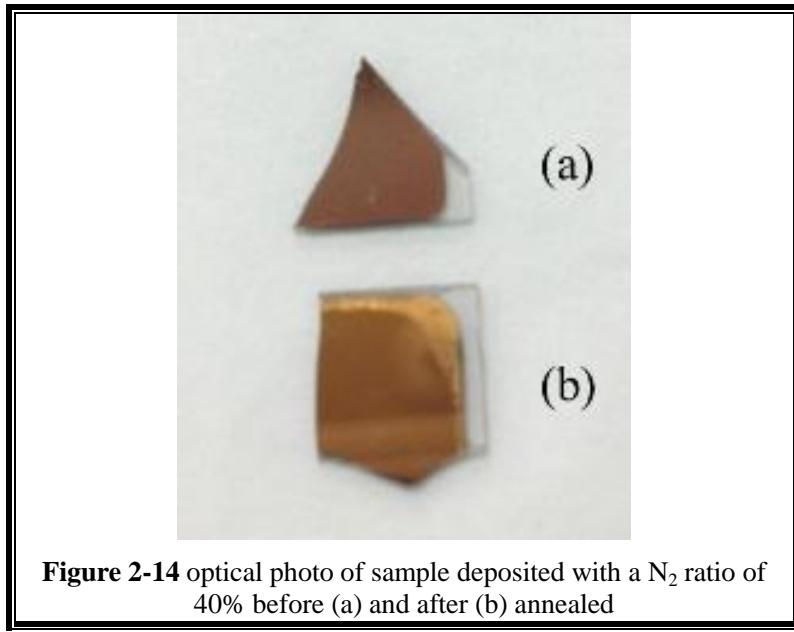


Figure 2-14 optical photo of sample deposited with a N_2 ratio of 40% before (a) and after (b) annealed

§2.6. Conclusion

We evaluated the thermal stability of different kinds of refractory metal nitrides as Schottky contact on GaN and chose TiN as the candidate electrode. Then, we deposited TiN films with different N_2/Ar ratios (nitrogen percentage). Higher nitrogen ration resulted in lower growth rate. Lower resistivity was obtained at medium nitrogen content. All the samples showed good rectifying properties with SBH of about 0.5 eV. Raman spectra implied the decrease of N vacancy concentration with increasing the nitrogen portion in source gas. Combined the Raman spectra and XPS results, the increase of the film resistivity after anneal was attributed to the oxidation and/or nitridation occurred in the film surface layer. Films deposited with medium nitrogen percentage showed the best film quality and thermal stability.

Chapter 3: GaN Schottky barrier diode with TiN electrode for microwave rectification

§3.1. Schottky barrier diode for microwave rectification

Wireless power transmission using microwave was developed fifty years ago.[36] Recently, it has been attracting much attention owing to the increasing demands for the various wireless technologies, such as electric vehicle power charging, energy harvesting,[37] ubiquitous power source,[38] and wireless power distribution within a building.[39] In the receiving terminal of a wireless power transmission system, which consists of DC/RF conversion, microwave transmission and RF/DC conversion, a so-called rectenna circuit is adopted to complete the RF to DC conversion.[40] The conversion efficiency strongly depends on the performance of the Schottky barrier diode (SBD) used in the rectenna circuit, such as on-resistance, off-capacitance, and turn-on voltage. To improve the efficiency, the reduction of the turn-on voltage to breakdown voltage ratio is very important.[41] As a wide bandgap semiconductor, gallium nitride (GaN) is regarded as a promising material compared with silicon and GaAs to realize high breakdown-voltage, low turn-on voltage to breakdown voltage ratio, and low-resistance devices.[42] However, the turn-on voltage of GaN SBD was about 0.8 V when a Ni electrode was adopted.[43] It is possible to reduce the turn-on voltage by using low work function metals.[44,45] In this case, attentions should be paid to suppress the leakage current due to the possible interface reaction. Other novel ideas are the proposals of using F-ion implantation[46] or recessed anode technique [47] to realize low turn-on voltage on AlGaN/GaN heterostructure and good results were achieved. Here, we propose an n^- -GaN/ n^+ -GaN structure to realize a quasi-vertical structure. By using this structure, low sheet resistance can be expected by adopting the n^+ -GaN access layer.

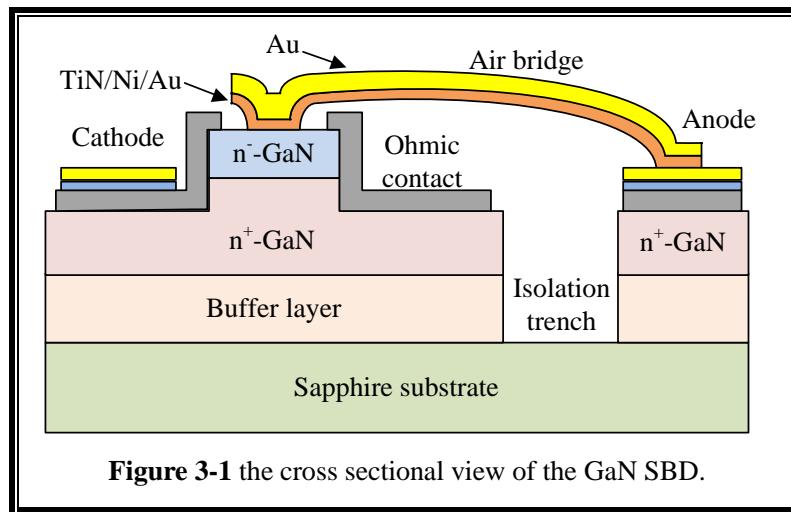
We have reported that good rectification characteristics could be obtained on GaN by reactive sputtering of some metals in a mixture gas ambient of Ar and N₂. Some metal nitrides, such as TiN, TaN, MoN, and MoSiN, are possible candidates to develop Schottky contact on GaN due to their favorable work functions, low resistivity, thermal stability, and compatibility with high- k dielectric. We have also found that TiN/W/Au gate stack structure on AlGaN/GaN heterostructure field-effect

transistors (HFETs) showed good thermal stability even at the temperature of 800 °C. In this paper, we will report GaN SBDs for microwave rectification with a low turn-on voltage by using reactively-sputtered TiN as the Schottky electrode.

§3.2. Fabrication of Schottky Barrier Diode with TiN Electrode

For film evaluation, TiN film with a thickness of 200 nm was formed on a sapphire substrate by reactive sputtering (DC, 75W) in Ar:N₂ (15:3 sccm) mixed gas atmosphere under 0.14 Pa, using a metal target of Ti with a purity of 99.99%. The average sputtering rate is about 0.61 nm/min and the resistivity of the film is about 1.6×10^{-4} Ωcm. The X-ray diffraction (XRD) spectrum of the sample (Figure 2-5) shows four peaks at 33.9 °, 35.9 °, 71.4 °, and 76.4 °. The peaks appear as a pair according to the radiation of Cu-K_α (right) and Cu-K_β (left). The first two and the next two peaks are corresponding to the TiN diffraction patterns of (111) and (222), respectively. Furthermore, the atomic force microscope (AFM) image of the film is shown in the Figure 2-8. The root mean square surface roughness is about 0.38 nm, which implicates the smooth surface. The nitrogen content determined by x-ray photoelectron spectroscopy (XPS) is about 84.5%.

The cross sectional view of the GaN SBD for microwave rectification is shown in Figure 3-1. The epi-wafers are grown on a *c*-plane sapphire substrate with a buffer layer, an n⁺-GaN access layer and an n⁻-GaN drift layer. The thickness and sheet resistance of the n⁺-GaN access layer is about 3.5 μm and 25 Ω/square, respectively. For the n⁻-GaN drift layer, the thickness is about 0.4 μm with an impurity density of 3×10^{17} cm⁻³.



The fabrication process started from the drift layer mesa formation by etching to the n⁺-GaN layer with inductively coupled plasma (ICP) dry etching. Deep trench isolation to the sapphire substrate was then conducted to reduce the pad capacitance of anode. After that, SiO₂ was deposited for surface protection. To form the cathode ohmic electrode, Ti/Al/Ni (30/120/40 nm) were deposited by sputtering followed by annealing at 850 °C for 1 min in N₂ ambient. The cathode electrodes were then thickened using gold electroplating. After cleaning in a BHF and a diluted HCl solution, TiN/Ni/Au (10/5/5 nm) thin film was deposited for anode Schottky electrode. For comparison, samples with Ni/Au (10/10 nm) electrode with an average sputtering rate of about 1.0 nm/min was also prepared by RF sputtering in Ar (30 sccm) gas atmosphere under a pressure of 0.14 Pa and a power of 10 W. Next, an Au film with thickness of about 1 μm was electroplated for the anode electrodes and the air-bridge interconnection. Finally, post-annealing at 300 °C was conducted for 10 min. A scanning electron microscope of a one-finger diode is shown in Figure 3-2.

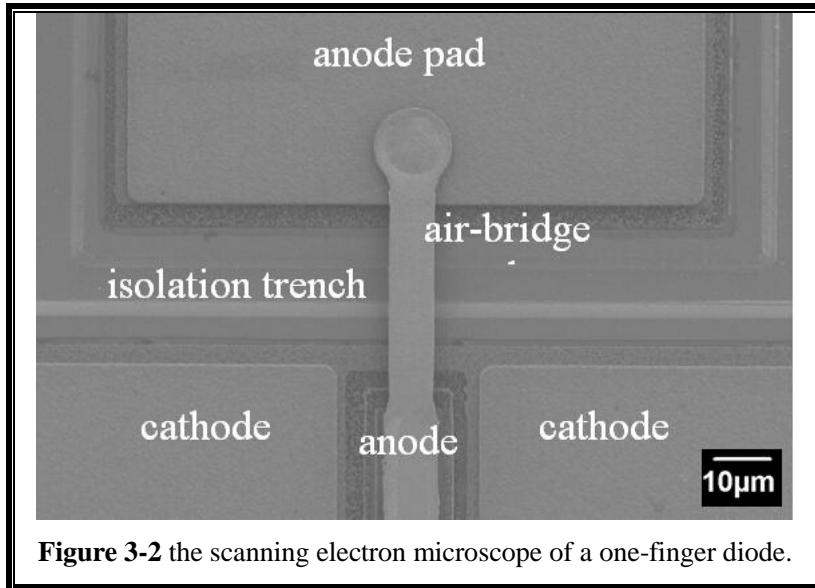


Figure 3-2 the scanning electron microscope of a one-finger diode.

§3.3. DC characterization of the Schottky barrier diode

Three types of diodes were designed to evaluate the electrical properties: circular-type (no air-bridge) with a radius of 60 μm for the evaluation of Schottky characteristics, finger-type with a length of 50 μm and width of 4 μm, and dot-type with a radius of 5 μm for microwave application. Figure 3-3 shows the current-voltage (*I*-*V*) characteristics of circular Schottky diodes with Ni and TiN contacts in logarithmic plot (a) and linear plot (b) in the forward region. Both of the

samples show good rectifying characteristics with curvature coefficients of about 33 and 36 for Ni and TiN, respectively (Figure 3-3a). The curvature coefficient γ is a diode figure of merit commonly used to quantify the detector capabilities of tunneling devices. A measure for the degree of diode nonlinearity normalized to the admittance level is calculated as the ratio of the second to the first derivative of the I - V characteristic [$\gamma=(d^2I/dV^2)/(dI/dV)$]. [48] Therefore, in classical (drift diffusion) pn junctions, $\gamma=1/kT\approx38 V^{-1}$.[49] The smaller calculated value is due to the relatively larger ideality factor in our diodes.

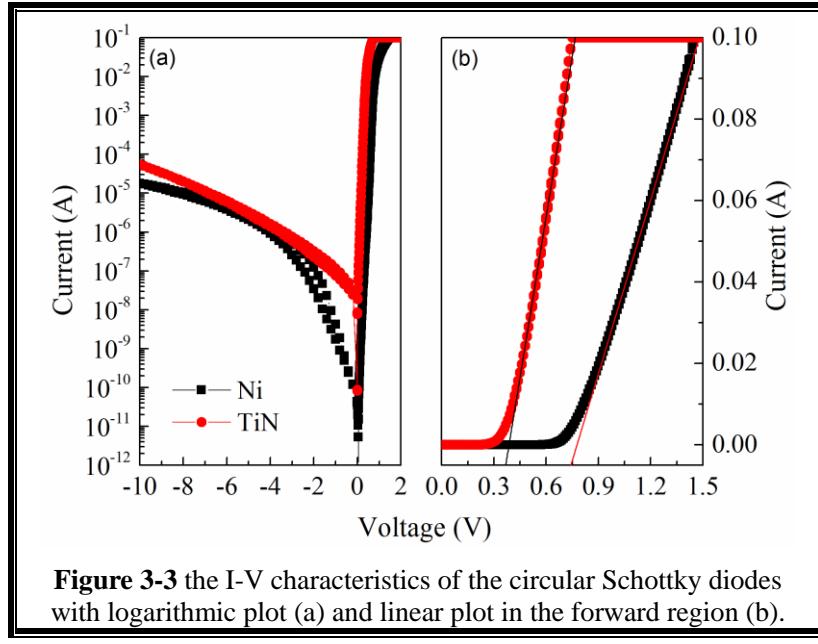


Figure 3-3 the I-V characteristics of the circular Schottky diodes with logarithmic plot (a) and linear plot in the forward region (b).

The Schottky barrier height (SBH) Φ_b and ideality factor n deduced from the circular-type diodes with TiN diode are around 0.59 eV and 1.07, respectively. On the other hand, they are around 0.87 eV and 1.23, respectively, for the Ni diode. Generally, the Ni has a higher work function (5.1 eV) than that of TiN (about 4.7 eV). The lower Schottky barrier height is attributed to the lower work function of TiN.[50] However, the reverse current leakage of Ni is just about 1~2 orders of magnitude lower than that of TiN diode, which is much higher than that calculated with the SBH of 0.87 eV. The increase of leakage current of the Ni diode is attributed to the interface states existing at the Ni/GaN interface caused by the interaction, leading to a defect-assisted tunneling effect.[51-53] The turn-on voltage, which is extracted by linear fitting the forward region (Figure 3-3b), is about 0.38 and 0.77 V for TiN and Ni electrode, respectively. The forward turn-on voltage for a Schottky rectifier is

given by $V_{on} = \frac{n k T}{q} \ln \left(\frac{I}{A A^* T^2} \right) + n \Phi_b + R_{on} I_{on}$ and the lower turn-on voltage of TiN is due to the relatively lower Φ_b when the on-resistance is comparable with Ni. [54]

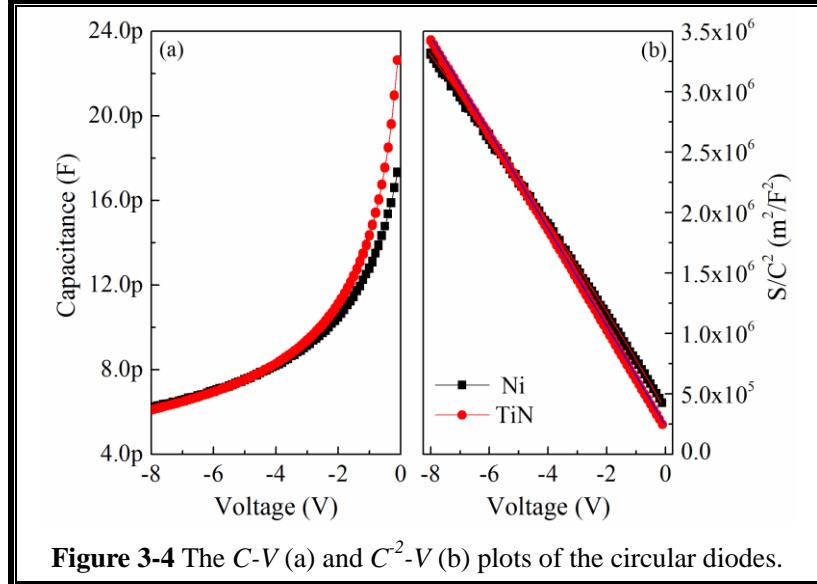


Figure 3-4 The C - V (a) and C^2 - V (b) plots of the circular diodes.

The corresponding capacitance-voltage (C - V) curves of the diodes are shown in Figure 3-4a. The capacitances obtained from the circular diode at zero bias are about 2.48×10^{-7} and 2.30×10^{-7} F/cm² for the TiN and Ni diode, respectively. C - V method is also a convenient and common method for evaluating the Schottky barrier height, by which the built-in potential V_{bi} can be extrapolated from the intercept in the voltage axis in the straight line of $1/C^2$ versus V . One critical assumption to adopt this method is that the carrier concentration in the semiconductor remains constant. It is inapplicable when the $1/C^2$ versus V plot is nonlinear due to the un-constant doping, such as during ion implantation, component diffusion or unintentional doping.[55] The carrier concentration profile of the samples, which was measured on the basis by standard C-V measurement, was found to be variable and exponentially increases with depth and can be fitted by $n(x) = N_0 e^{\alpha x}$, where α is a fitting constant, x is the distance from the surface and N_0 is the carrier concentration at the interface. Figure 3-4b shows the measured and fitted carrier concentration profiles of Ni diode ($N_0 = 3.39 \times 10^{17}$ cm⁻³, $\alpha = 2.7 \times 10^{-3}$ cm⁻¹) and TiN diode ($N_0 = 3.50 \times 10^{17}$ cm⁻³, $\alpha = 5.0 \times 10^{-4}$ cm⁻¹). The exponential carrier profile is due to the unintentional doping of the sample by the MOCVD technique, where the doping comes mainly from the residual impurities and the defects. The impurities and defects decrease from the bottom towards the top

during growth. Using the carrier concentration profiles shown above and the derivation method described in ref. 55, the ϕ_b of Ni and TiN measured from the capacitance-voltage curves are about 0.84 and 0.60 eV, respectively. They are coincident with that derived from *I-V* characteristics.

Similar results were obtained for the finger- and dot-type SBDs, which are designed for microwave rectification by reducing the Schottky contact area. The *I-V* characteristics of the dot-type Schottky diodes with TiN and Ni electrode are shown in Figure 3-5, with an on-resistance of 9.0 and 11.0 Ω , respectively. To verify the dependence of turn-on voltage upon the device type, the logarithmic and linear plots of the forward *I-V* characteristics of three types of TiN SBDs are shown in Figure 3-6. Obviously, all types of TiN SBDs show good rectifying characteristics. The circular-type SBD shows a relative lower saturation current density at high voltage due to the larger area. However, the extracted turn-on voltages for the circular-, finger-, and dot-type SBDs are around 0.38, 0.50 and 0.56V, respectively, showing slight dependence on device type.

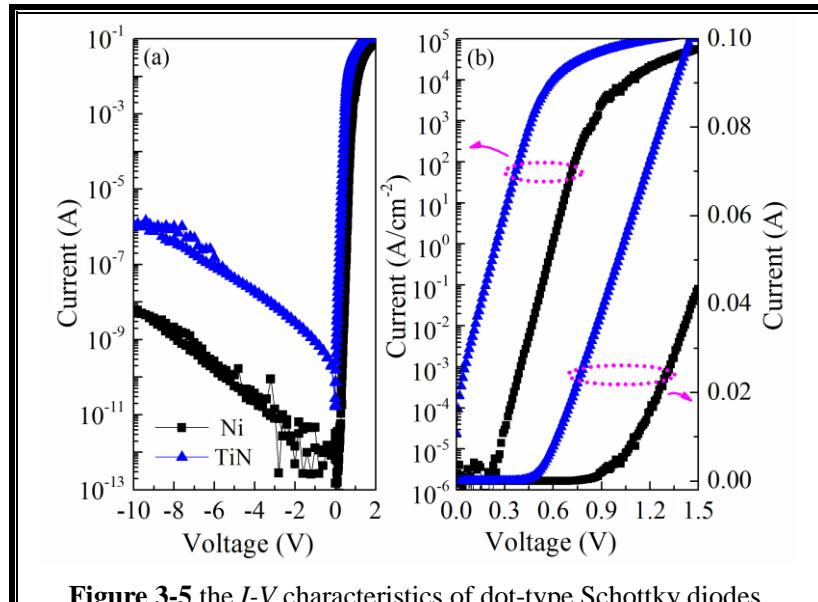


Figure 3-5 the *I-V* characteristics of dot-type Schottky diodes.

The experimental *I-V* data of Schottky contact can be analyzed by the thermionic emission equation with series resistance. At forward-bias, the *I-V* characteristic is given as follows:[56]

$$I = A_e A^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \left[\exp\left(\frac{qV - qIR_s}{nkT}\right) - 1 \right], \quad (3-1)$$

And it can be wrote as:

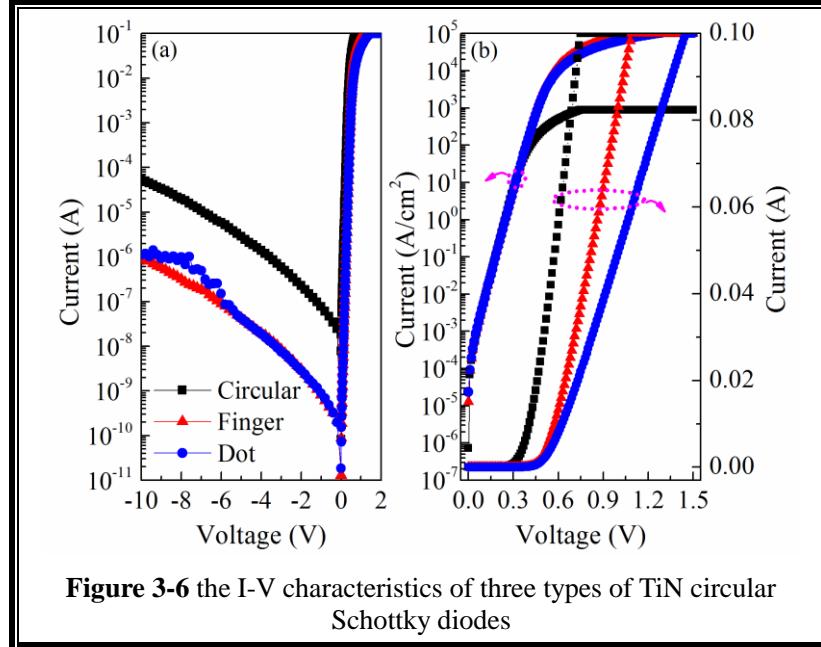
$$V = \frac{1}{K_2} \ln \left(\frac{I + K_1}{K_1} + K_3 I \right)$$

$$K_1 = A_e A^* T^2 \exp \left(-\frac{q \phi_b}{kT} \right), \quad (3-2)$$

$$K_2 = \frac{q}{nkT}$$

$$K_3 = \frac{qR_s}{nkT}$$

where A_e is the effective diode area, A^* the effective Richardson constant of GaN, T the absolute temperature, q the electron charge, V the forward-bias voltage, k the Boltzmann constant, Φ_b the experimental zero-bias apparent barrier height and n the ideality factor.



We first fit the I - V curves of TiN Schottky diodes with the equation (3-2) shown above. It shows that the Schottky barrier heights of the three samples are similar (about 0.6 eV), while the ideality factor (1.11, 1.15, and 1.17) and the series resistance (3.1, 5.0, and 8.4 Ω) increases with the area decreasing for the three diodes (Figure 3-7). To evaluate the effect of each parameter, we assume the barrier height (0.6 eV) and the series resistance (10Ω) as constant and change the ideality factor (1.0, 1.1, 1.2), it can be understood that increasing of the ideality factor can cause the increase of turn-on voltage. On the other hand, assuming the barrier height (0.6 eV) and the ideality factor (1.0) as constant and changing the series resistance (10, 20, 30 Ω), it

indicates that the increasing series resistance can cause the decrease of current density, while the turn-on voltage extracted by linear fitting the forward region nearly is independent on the series resistance (Figure 3-8). So the increased ideality factor is responsible for the turn-on voltage increasing. The geometry-dependence of the ideality factor is considered to relate with the surface treatment before the anode metal deposition. It may become more difficult to clean the surface perfectly when the area is small.

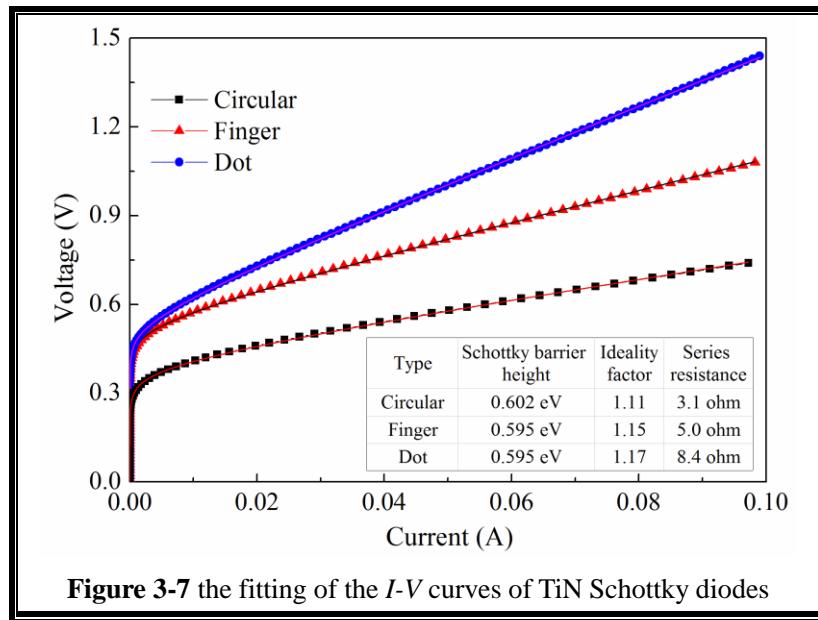


Figure 3-7 the fitting of the I - V curves of TiN Schottky diodes

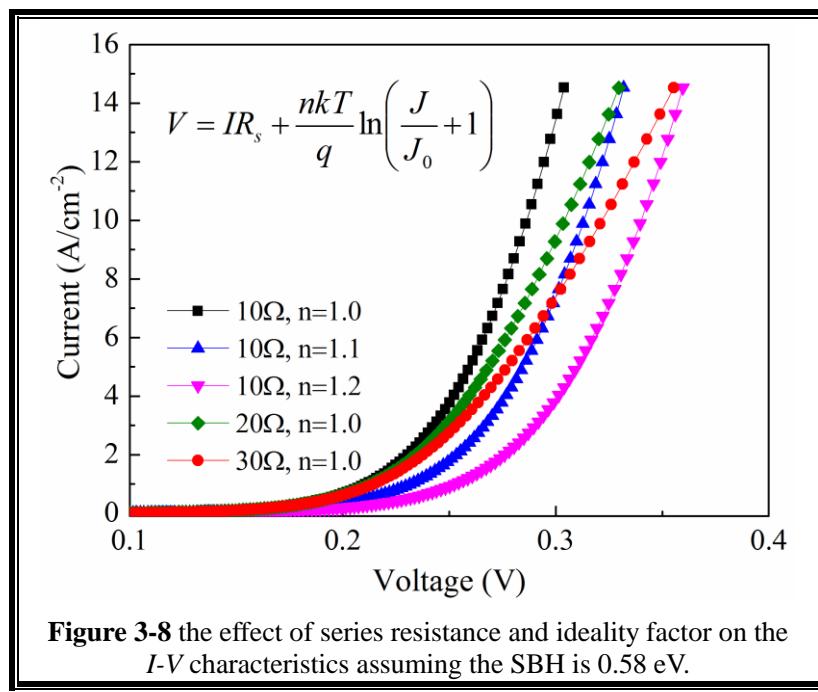


Figure 3-8 the effect of series resistance and ideality factor on the I - V characteristics assuming the SBH is 0.58 eV.

For a comparison, the linear plots of the forward I - V characteristics of three types of Ni SBDs are shown in Figure 3-9. Obviously, the extracted turn-on voltages for all types of Ni SBDs also show slight dependence on device type. By fitting the I - V curves of Ni Schottky diodes with the equation (3-2), It shows that the series resistance (6.1, 12.2, and 12.3 Ω) increases with the area decreasing for the three diodes, while the Schottky barrier heights and the ideality factor of the three samples are varying. This may be attributed to the interface states existing at the Ni/GaN interface caused by the interaction, leading to a defect-assisted tunneling effect and deviation from the thermionic emission equation, especially for the dot-type SBDs.

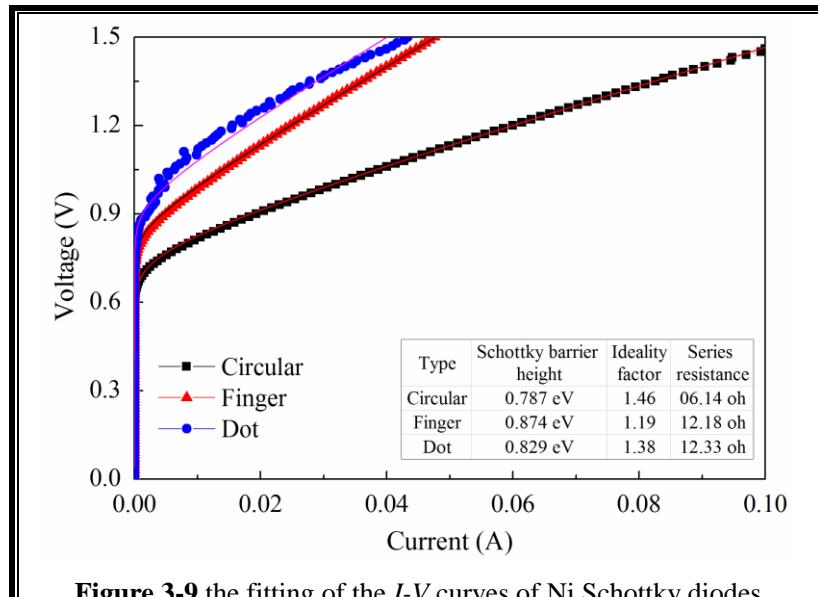


Figure 3-9 the fitting of the I - V curves of Ni Schottky diodes

The breakdown voltage (V_{BK}) of the dot-type diode is defined as the voltage corresponding to a sudden leakage current reduction, which is regarded as the breakdown point. The measured V_{BK} is about 40 V for both the TiN and Ni diode, as shown in Figure 3-10. Furthermore, the breakdown voltage can be enhanced to about 90 V for the TiN diode fabricated on 1 μm thick drift layer with an impurity density of $1 \times 10^{17} \text{ cm}^{-3}$. It is also compatible with our reported result of the Ni diode which was fabricated on a wafer with a similar drift layer thickness and impurity density. In our structure, the epi-wafers are consist with a buffer layer, an n^+ -GaN access layer (impurity density over $4 \times 10^{18} \text{ cm}^{-3}$) and an n^- -GaN drift layer (impurity density is about $3 \times 10^{17} \text{ cm}^{-3}$). The thickness of the n^+ -GaN access layer and n^- -GaN drift layer is about 3.5 μm and 0.4 μm , respectively. Under the reverse bias, the n^- -GaN drift layer

will be depleted but the depletion layer of the n⁺-GaN access layer can be ignored due to the extremely high impurity density. In this case, the breakdown is determined by the thickness of the n⁻-GaN drift layer. Theoretically, the breakdown voltage (V_{BD}) of the diode can be given as $V_{BD} = \frac{1}{2}W_D E_c$. Assuming the critical electric field (E_c) of the GaN is about 2×10^6 V/cm and the depletion width (V_{BD}) is about 0.4 μm, the calculated breakdown voltage is about 40 V. [57]

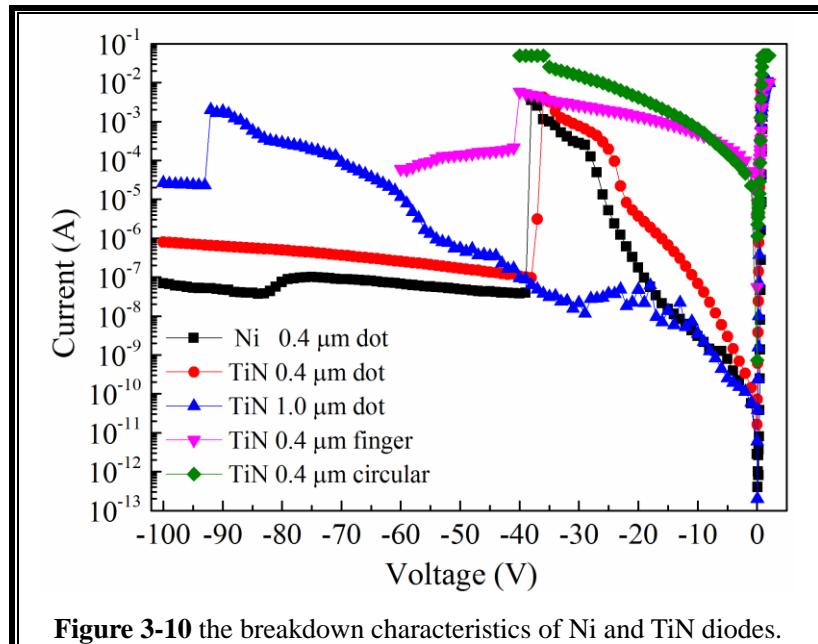


Figure 3-10 the breakdown characteristics of Ni and TiN diodes.

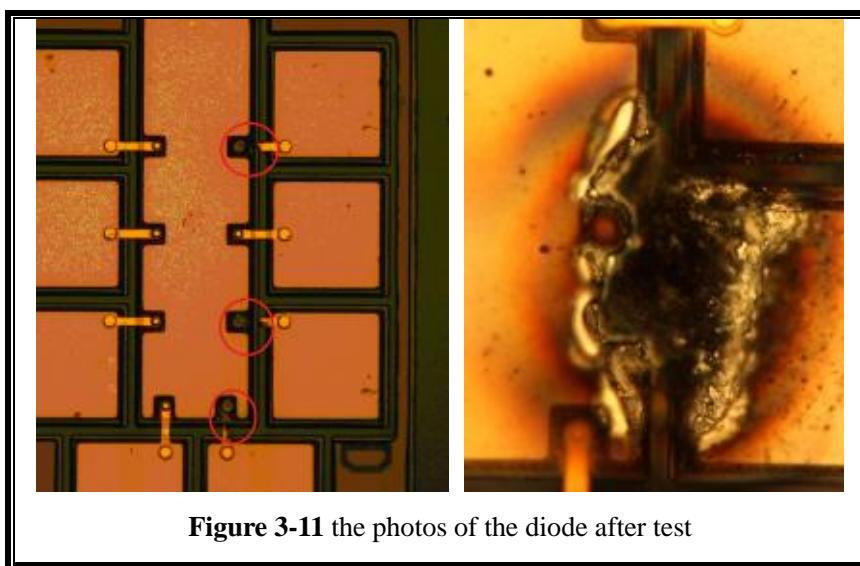


Figure 3-11 the photos of the diode after test

The breakdown occurred in the anode side due to the fusing of the anode side as shown in the optical photos (marked in the red circle of Figure 3-11). The left one is

corresponding to the sample TiN-0.4 μm and the right one is to the sample TiN-1.0 μm . The sample measured at higher voltage may cause more serious damage on the devices. After breakdown, the current in both the forward region and the reverse region decreased. It is clear that the TiN diode has the similar breakdown voltage but a nearly half of the turn-on voltage comparing with the Ni diode, resulting in a reduction of the turn-on voltage to breakdown voltage ratio.

§3.4. RF characterization of the Schottky Barrier Diode

Figure 3-12 shows the measured Y-parameters obtained from S-parameter measurement of a finger-type diode as a function of bias voltage. The TiN diode shows a higher susceptance at reverse bias (Figure 3-12a). The conductance rises at about 0.33 and 0.75 V (Figure 3-12b), which is consistent with the DC measurement. Assuming that the reflection is zero, microwave power is 1W and the load is 50 Ω , we calculated that the efficiency of a rectenna circuit at 2.45 GHz can be enhanced from 84% to 89% when the turn-on voltage decreases from 1.0 to 0.5 V (Figure 3-13).

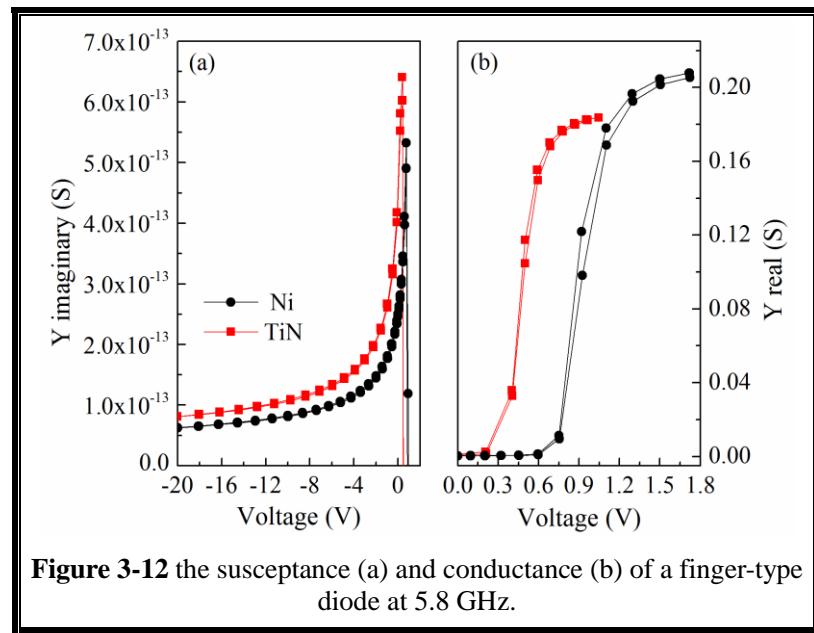
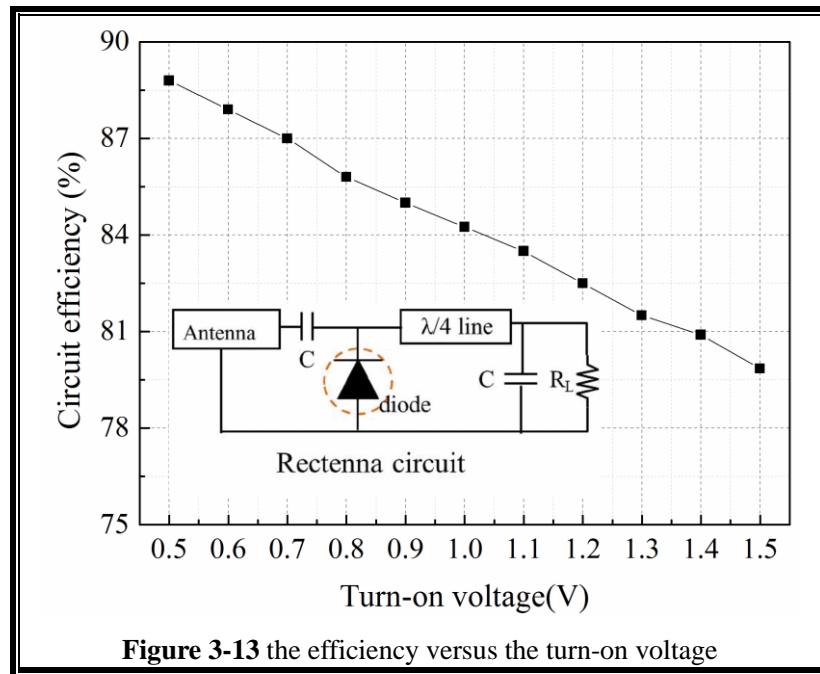


Figure 3-12 the susceptance (a) and conductance (b) of a finger-type diode at 5.8 GHz.

**Figure 3-13** the efficiency versus the turn-on voltage

§3.5. Conclusion

GaN SBDs with TiN electrode were developed to realize low turn-on voltage for microwave rectification. The average turn-on voltage (on-resistance) of the TiN diode is about 0.38 V ($9.0\ \Omega$) as compared with 0.77 V ($11.0\ \Omega$) of Ni. Three types of TiN SBDs were fabricated to verify the dependence of turn-on voltage upon the device type. The Schottky barrier height is comparable to each other while the extracted turn-on voltages for the circular, finger, and dot type SBDs are around 0.38, 0.50 and 0.56V, respectively. This may be attributed to the increase of the ideality factor of the diode when decrease the electrode area. Beside of this, the TiN diode kept the same level in breakdown voltage of about 40 V. Based on these results, the calculated efficiency of a rectenna circuit at 2.45 GHz can be enhanced from 84% to 89% by using TiN-based GaN SBDs.

Chapter 4 : The fabrication of AlGaN/GaN HFETs with a self-aligned-gate process

§4.1. The self-aligned-gate process

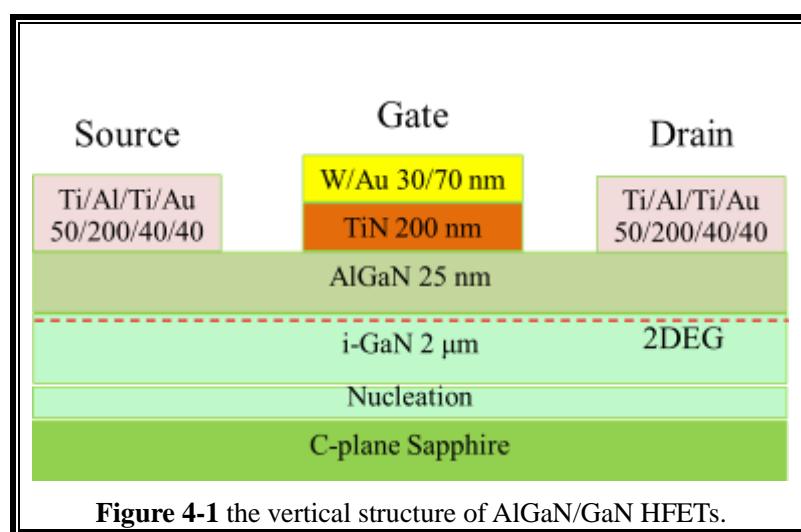
Gallium nitride (GaN) and its related AlGaN/GaN heterostructure field-effect transistors (HFETs) have been widely developed for application in the area of high-frequency, high-power and high-temperature owing to the wide bandgap, low intrinsic carrier concentration, high electron mobility and high saturation velocity. [58,59] Conventional fabrication processes of the HFETs involve patterning and annealing the source and drain contacts before the formation of the Schottky gate contact because annealing at relatively high temperature is necessary to obtain Ohmic contact. After the formation of the Ohmic contact, gate electrode is then patterned and deposited by aligning the Ohmic patterns. Due to the alignment process, this approach limits the minimum source-to-gate and drain-to-gate distances and makes it very difficult to obtain small access resistances. Alternatively, a self-aligned-gate (SAG) process is proposed, in which a T-shaped Schottky gate is fabricated and then used as a mask directly for the Ohmic metal evaporation. Then, the Schottky gate and the Ohmic electrodes are annealed simultaneously to achieve Ohmic contacts. This technology is actually a so-called gate-first process.[60] The SAG structure can reduce the source and drain access resistance further by reducing the spacing among the electrodes.[61] The important technologies to form the SAG structure are the formation of T-gate and the Schottky gate structure which can stand the Ohmic annealing process. Usually, Ti-based complex multilayer systems such as Ti/Al/Ni/Au, Ti/Al/Ti/Au, Ti/Al/Pd/Au and Ti/Al/Mo/Au are widely used to form Ohmic contacts on n-type GaN and AlGaN/GaN HFETs.[62] However, to form the Ohmic contact with Ti-based multilayers on GaN-based materials, the formation of a metallic compound and nitrogen vacancies are needed, which show great dependence on the annealing temperature (commonly above 700°C). Therefore, an appropriate gate stack that can withstand such a high ohmic annealing temperatures is necessary for fabricating SAG devices. However, the recent Ni or Cu gate materials on AlGaN/GaN HFETs could not stand the Ohmic annealing temperature. [63,64]

Refractory metal nitrides, such as WN, TiN, TaN, MoN, TaSiN, and MoSiN, are

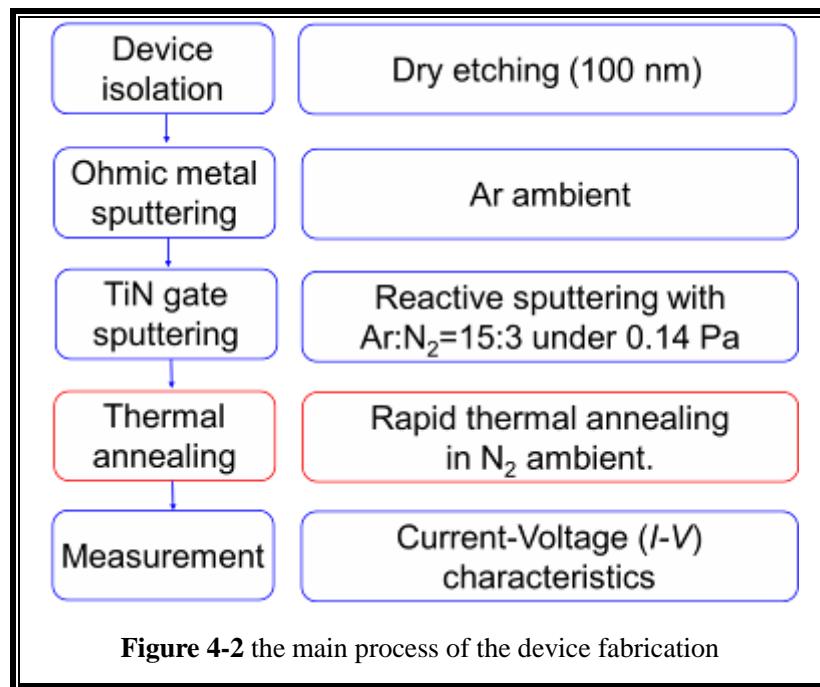
ideal candidates to develop this structure due to their favorable work functions, low resistivity, thermal stability and compatibility with high- k dielectric. In our previous reports, we found that TiN showed good thermal stability even at the temperature of 850°C. The resistance of metal nitride was found to be much higher than that of metal itself. A stack gate structure with Au top layer is necessary to reduce the electrode resistance. In this chapter, to develop a gate-first process for application in the SAG structure, we proposed a stack gate structure on AlGaN/GaN HFETs by applying TiN as the gate contact material and W/Au as a cap layer to reduce the gate resistance. As an evaluation method of the gate-first process, we deposited the ohmic metals firstly followed by the deposition of gate electrodes. The deposited ohmic and gate electrodes were then annealed together by changing the annealing temperature and annealing time. The effects of the annealing process on the device performances were evaluated.

§4.2. Device for the self-aligned-gate process evaluation

The epitaxial layers of the AlGaN/GaN HFETs were grown by metal organic chemical vapor deposition (MOCVD) on a c-plane sapphire substrate as shown in Figure 4-1. The heterostructure consisted of a nucleation layer, a 2 μm undoped GaN channel layer, and a 25 nm undoped AlGaN layer from bottom to top. The Al mole fraction of the AlGaN layer was 24%. From the Hall measurement at room temperature, the mobility and average sheet resistance of the two-dimensional electron gas (2DEG) are 1665 cm²V⁻¹s⁻¹ and 412 Ω/□, respectively.



The device fabrication (Figure 4-2) started with mesa isolation which was formed by inductively coupled plasma (ICP) with the etching depth of 100 nm. Ohmic contact metals were then deposited which were consisted of Ti/Al/Ti/Au (50/200/40/40 nm). After gate pattern lithography, the samples were treated by O₂ plasma ashing as surface cleaning and then immersed in diluted HCl (HCl:H₂O=1:1) for over 5 min to remove the native oxide layer. TiN films (about 200 nm) were formed by DC magnetron reactive sputtering in Ar and N₂ ambient (Ar:N₂=15:3 sccm) under 0.14 Pa, using target metal of Ti with a purity of 99.99%. After that, a cap layer of W/Au (30/70 nm) was deposited on the TiN layer in Ar ambient to reduce the gate resistance. Finally, the samples were divided into two groups for annealing process. One group of the samples with non-annealed ohmic and Schottky contacts were annealed under 750, 800, 850 and 900 °C for 1 minute simultaneously. In another group, the samples were annealed under 800 °C for 0.5, 3, 5 and 10 minutes. The electrical properties of the devices were evaluated systematically.



§4.2.1. The effect of annealing temperature on the gate

The XRD spectra of the samples on sapphire after normalized (111) peak (Figure 4-3) show four peaks at 33.9 °, 35.9 °, 71.4 °, and 76.4 °. The peaks appear as a pair according to the radiation of Cu-K_α (right) and Cu-K_β (left). The first two and the next two peaks are corresponding to the TiN diffraction patterns of (111) and (222),

respectively. Furthermore, the atomic force microscope (AFM) image of the film is shown inset of Figure 4-3. The root mean square surface roughness is about 0.38 nm, which implicates the smooth surface.

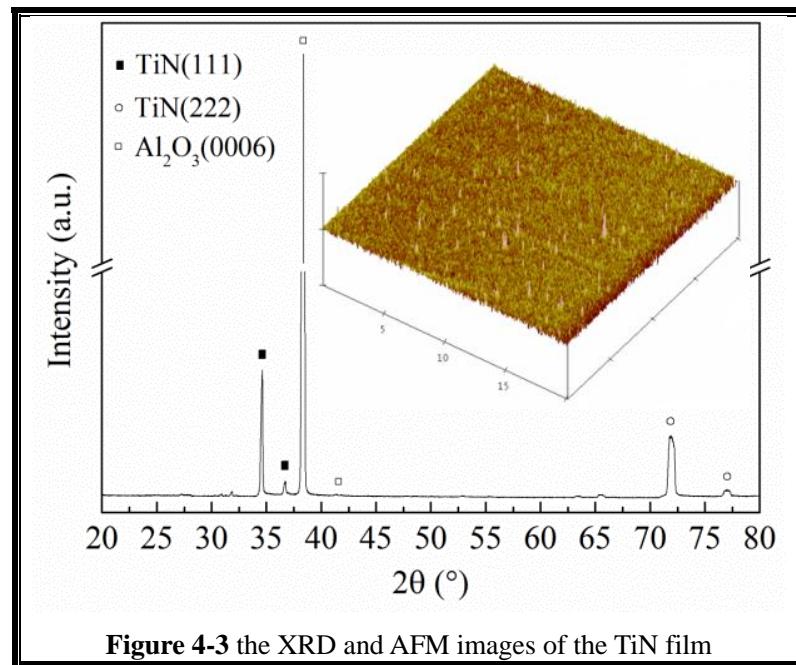


Figure 4-3 the XRD and AFM images of the TiN film

Transmission Line Model (TLM) is the commonly used method to assess the electrical properties as well as the quality of the ohmic contact. A schematic diagram of the TLM test structure is shown in Figure 4-4.

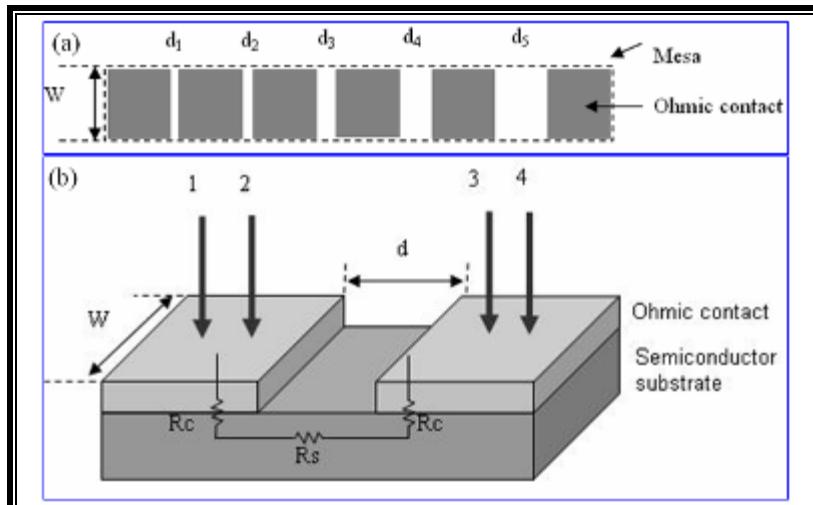


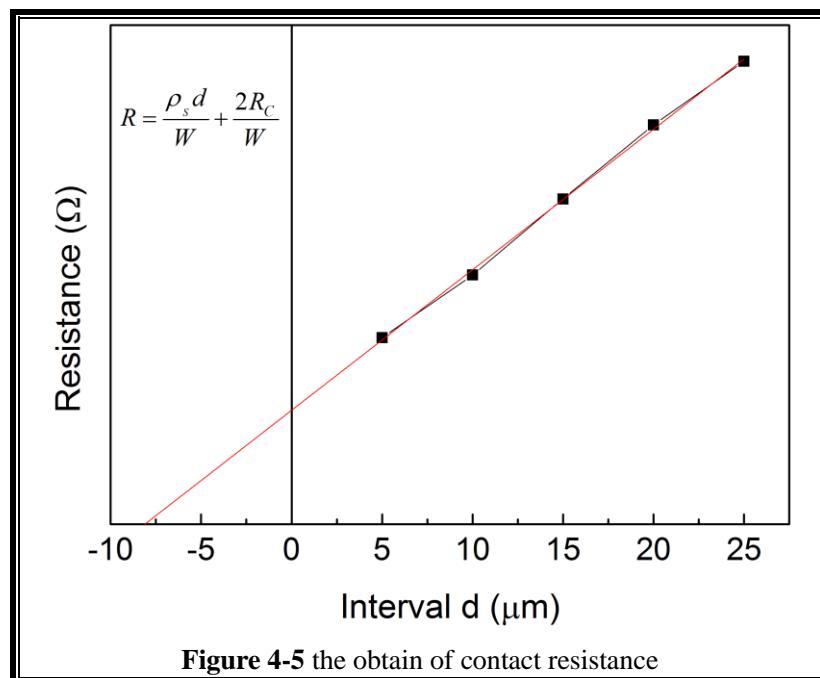
Figure 4-4 a schematic diagram of the TLM test structure

It consists of rectangular metal contact pads with spacing between them are $d=5$,

10, 15, 20, 25 μm , respectively. The length L and width W of the contact pad are 1mm and 100 μm . To obtain an accuracy measurement, the rectangular TLM test patterns were fabricated in the mesa-isolated area. This is because the mesa structure can eliminate the lateral current flows from one contact to the other contact, resulting in confining the current flow direction perpendicular to the edge of the metal contacts within one mesa. The four point probe method is used to measure the total resistance between two neighbouring pads separated by a distance d and is given by

$$R = \frac{\rho_s d}{W} + \frac{2R_c}{W}, \quad (4-1)$$

Where ρ_s and R_c are the semiconductor sheet resistance between the contact pads and ohmic contact, respectively. All voltage-drops in the horizontal direction are attributed to the current flow in ρ_s while the voltage drop in the vertical direction, perpendicular to the plane of the current is due to R_c . By plotting R as a function of d, a linear fit to the data as shown in Figure 4-5 can be made. From the slope and intercept, the ρ_s and R_c can be calculated. In order to normalize the contact resistance, the value of R_c is multiplied with W to obtain a value in $\Omega\cdot\text{mm}$.



The ohmic contact resistance (R_c) and wafer sheet resistance R_{wafer} at different annealing temperature and time were measured by transmission line model (TLM).

The sheet resistance of the gate film (R_{film}) was measured by four point probe method using a bridge resistor. As shown in Figure 4-6, after annealed at 750 °C for one minute, ohmic behavior was formed between the metal stack and the semiconductor though with a high contact resistance of about 2.96 Ωmm. The R_c then reduced rapidly to a minimum value of about 0.66 Ωmm when annealed at 800 and 850 °C. Further increasing the temperature to 900 °C, it slightly increased again. There was no obvious change on the wafer sheet resistance R_{wafer} after annealing (inset of Figure 4-6). The variation of the wafer sheet resistance may be related to the inhomogeneity of the wafer itself and the surface state change. While for the gate film resistance R_{film} , it accreted slowly from about 0.46 to about 0.48 Ω/□ first and suddenly tripled to about 1.29 Ω/□.

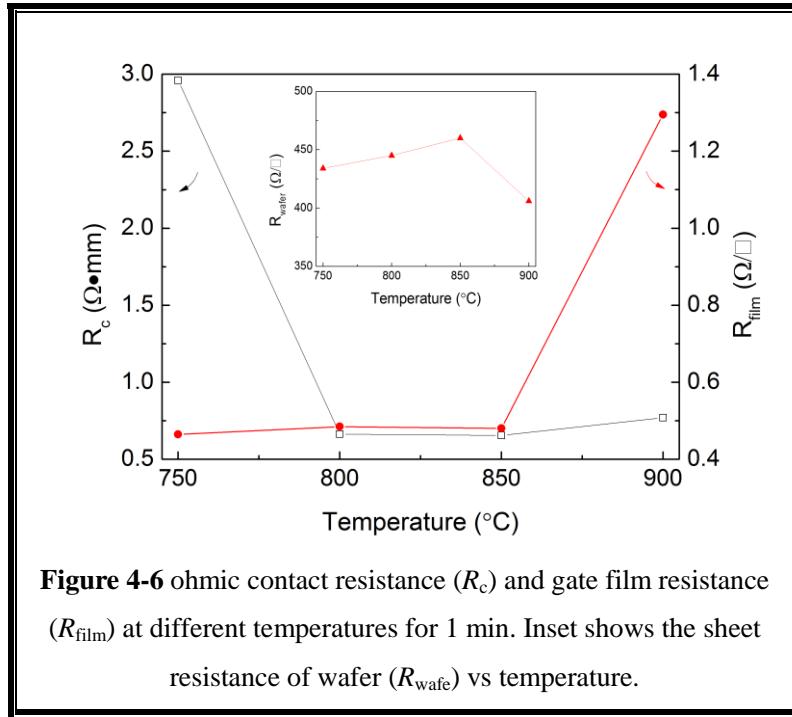


Figure 4-6 ohmic contact resistance (R_c) and gate film resistance (R_{film}) at different temperatures for 1 min. Inset shows the sheet resistance of wafer (R_{wafer}) vs temperature.

Generally, the mechanisms of forming an ohmic contact on AlGaN/GaN are the formation of N-vacancies and/or the lowering of the Schottky barrier (SB) via intermediate metallic compounds. For the Ti/Al-based multilayer structures, Ti reacts with GaN forming TiN intermetallic phase at elevated temperatures due to an exchange reaction mechanism, which can generate N-vacancies and create a highly doped region at the interface. Also, the diffusion of Al atoms through the Ti layer to form the low work function Al-Ti alloy is also benefit to obtain low resistance. [65,66]

Based on this, when the annealing temperature is low to some extent, the reaction between Ti and AlGaN is not sufficiency, the ohmic contact property becomes poor and the specific contact resistance becomes high. When the annealing temperature increases beyond the critical value ($850\text{ }^{\circ}\text{C}$ in our case), the intensive intermetallic diffusion have occurred. In-diffusion of Au towards AlGaN interface and out-diffusion of Al towards the contact surface may be the possible cause of the degradation of the contact characteristics. For the gate film, the increased resistance may be ascribed to the oxidation of non-nitridized Ti in the film by the residual oxygen in the nitrogen ambient during rapid thermal annealing (RTA) process. Beside of this, the ball-up of Au cap layer at $900\text{ }^{\circ}\text{C}$ as confirmed by optical micro-spectroscopy (Figure 4-7b) resulted in a rough surface and deteriorated the interface contact, causing the drastically increase of resistance.[\[67\]](#) For comparison, the gate morphology at $750\text{ }^{\circ}\text{C}$ remained very good, as shown in Figure 4-7a.

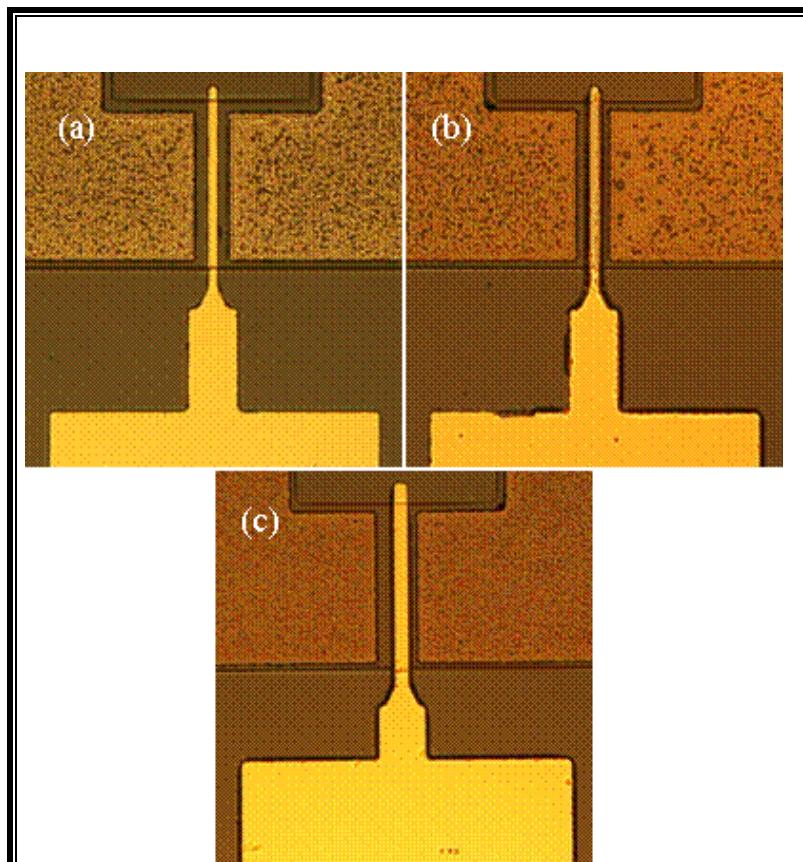


Figure 4-7 the optical photos for the samples annealed at $750\text{ }^{\circ}\text{C}$ for 1 min (a), $900\text{ }^{\circ}\text{C}$ for 1 min (b) and $800\text{ }^{\circ}\text{C}$ for 10 min (c).

Figure 4-8a shows the current-voltage (I-V) curves of circular TiN/W/Au Schottky diodes with diameter of 150 μm under different annealing temperatures. Obviously, the sample shows good rectification characterization even after annealed at all the temperatures. At 750 °C, the reverse leakage current is about 10^{-5} A. However, the reverse leakage current and the forward current at low forward bias increased when annealed at higher temperature. The later was considered to be due to the generation-recombination current and the tunnel current through the barrier.[68,69] It is found in Figure 4-8b that the forward current shows slight lower when annealed at 750 and 900 °C, which can be ascribed to the higher resistance of the ohmic and TiN/W/Au gate as described in Figure 4-7, respectively.

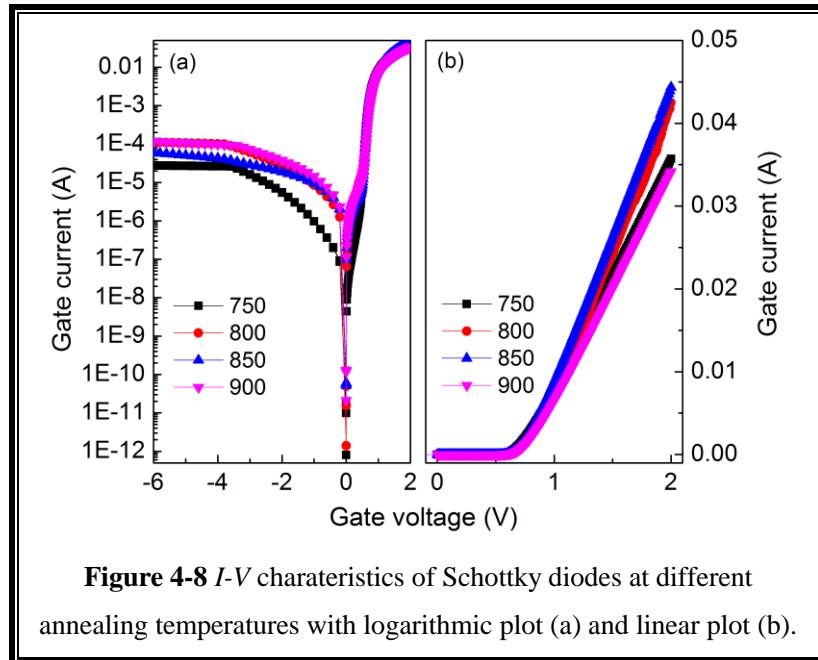


Figure 4-8 I-V characteristics of Schottky diodes at different annealing temperatures with logarithmic plot (a) and linear plot (b).

The corresponding capacitance-voltage (C - V) curves of the diodes are shown in Figure 4-9a. Obvious threshold voltage shift was not observed for all the samples. When the negative bias are below the threshold voltage (about -4.0 V), which is called as the sub-threshold region, the capacitance is very small depending on the anode-cathode distance because the background doping in the semi-insulating GaN layer is very low. Above the threshold voltage then, a capacity platform comes out which is determined by the total capacitance of the AlGaN layer. The slight decrease in the capacitance is due to the increase of series resistance when negative bias was applied. The capacitance was about 75 pF for sample annealed at 750 °C, and

increased to about 80 pF for samples annealed at 800 and 850 °C, finally became about 90 pF after annealed at 900 °C, implying the change of the total thickness. This may be ascribed to the disappearance of the natural oxide on the AlGaN layer and the interface reaction between the gate metal and the AlGaN layer.[70] When the bias voltage is positive and overcomes a critical value (about 0.5 V), the positive leakage current of the Schottky diode becomes so high that the equivalent model of calculating capacitance is not available. [71,72]

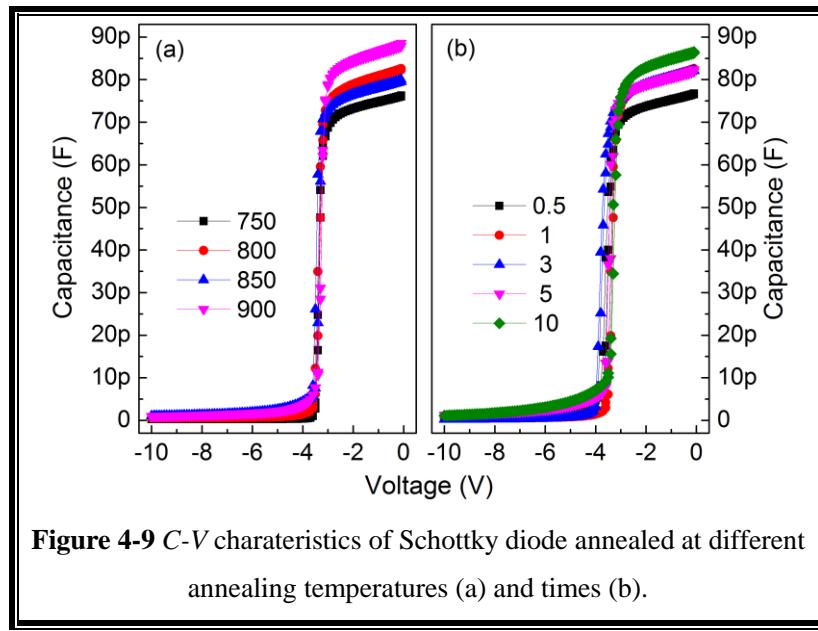


Figure 4-9 C - V characteristics of Schottky diode annealed at different annealing temperatures (a) and times (b).

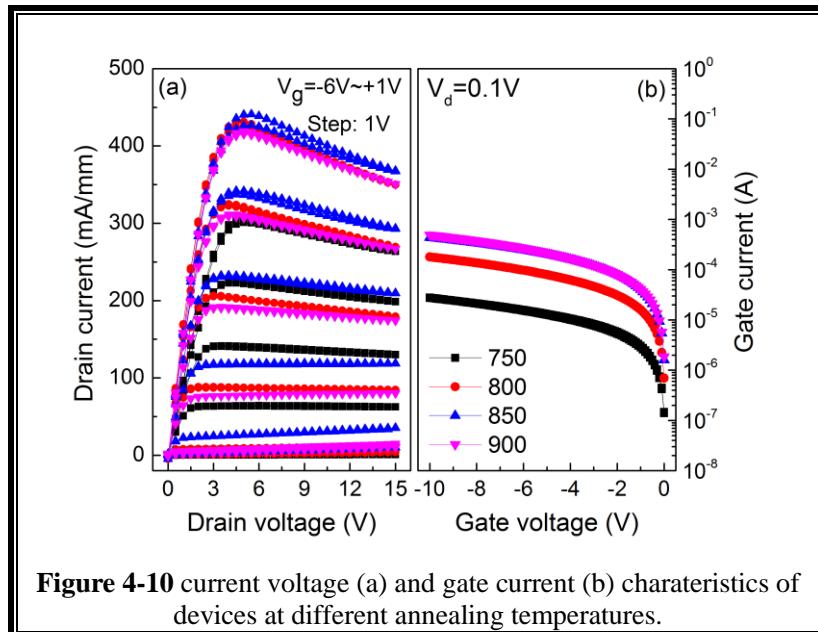


Figure 4-10 current voltage (a) and gate current (b) characteristics of devices at different annealing temperatures.

Figure 4-10 shows the influence of annealing temperature on *I-V* characteristics of the AlGaN/GaN HFET devices with gate length and gate-source/drain spacing of 3 and 3 μm , respectively. The gate voltage is swept from -6 to +1 V. All of the devices can operate well with the saturation current exhibiting a negative conductance at large drain voltage. The decrease in drain current at higher drain-source voltage is due to the self-heating and the decreased electron mobility. For the sample annealing at 750 $^{\circ}\text{C}$, the on-resistance is high and the maximum drain current is only 300 mA/mm due to the large Ohmic contact resistance. After annealing at 800, 850, and 900 $^{\circ}\text{C}$, the maximum drain current is increased to about 450 mA/mm and the on-resistance is also decreased. This phenomenon of drain current change is also confirmed from the temperature dependence of transfer characteristic and transconductance (Figure 4-11). However, the gate leakage current also increased when annealed at high temperature (Figure 4-10b). This increased of gate leakage can be also contributed to the disappearance of the natural oxide on the AlGaN layer and the interface reaction between the gate metal and the AlGaN layer, which can result in the increase of defect density which assists the carrier tunneling. [73]

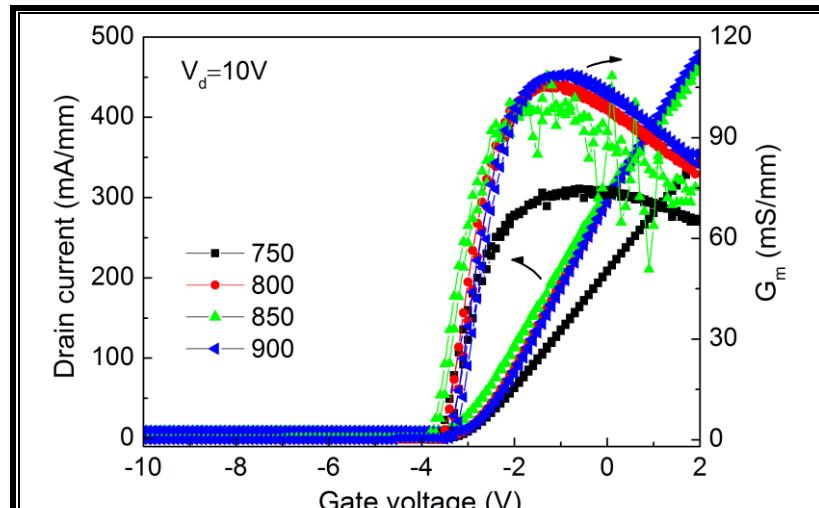


Figure 4-11 transfer characteristics of devices at $V_d=10$ V vs annealing temperature.

§4.2.2. The effect of annealing time on the gate

To evaluate the annealing time dependence of the fabricated AlGaN/GaN HFETs with TiN/W/Au gate, the devices were thermally treated in N_2 ambient with annealing temperature of 800 $^{\circ}\text{C}$, the temperature at which best ohmic contact was achieved in

the above experiments, for various times. The annealing time can also affect the contact resistance as plotted in Figure 4-12. Appropriate contact resistance of about $0.7 \Omega\text{mm}$ only can be obtained under mediate time of one and three minutes while the sheet resistance of the gate film accreted steadily from about 0.47 to about $0.67 \Omega/\square$ with the prolonging of time. This result implied that short annealing time caused the deficient reaction and long annealing time caused over-interdiffusion for Ohmic contact, respectively. It is worth noting that the increment of film resistance with longer time is smaller than that with higher temperature. As shown in Figure 4-7c, the gate morphology of the sample annealed at 800°C for 10 minutes remained very good, meaning that the ball-up of the cap metal layer at high temperature should be responsible for the increase of film resistance.

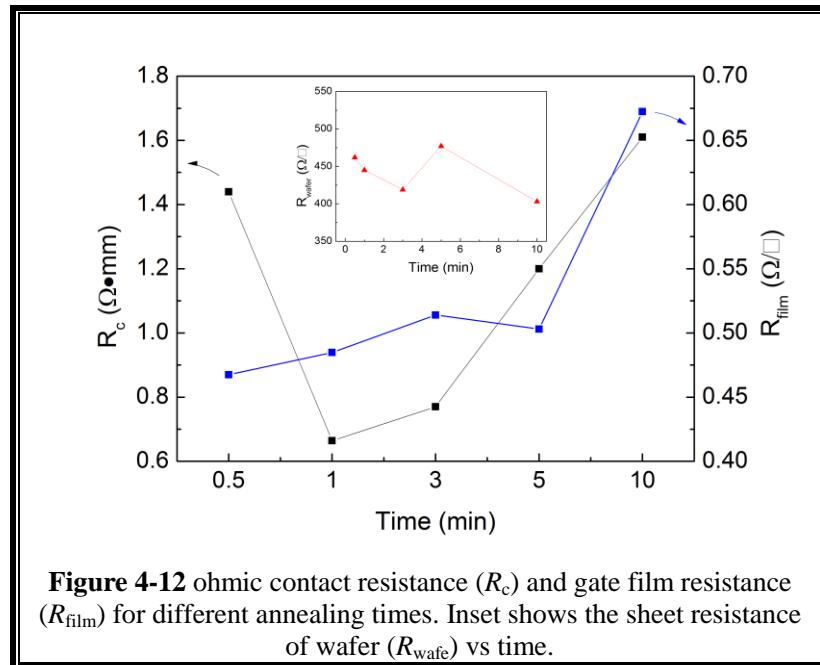


Figure 4-12 ohmic contact resistance (R_c) and gate film resistance (R_{film}) for different annealing times. Inset shows the sheet resistance of wafer (R_{wafe}) vs time.

Figure 4-13a shows the I - V characteristics of diodes with TiN/W/Au gate stack at different annealing times. All the samples show good rectification characterization though slight positive shift on threshold voltage was observed with the annealing time increasing. Prolonging the annealing time also resulted in the increase of both reverse leakage current (from $\sim 10^{-5}$ to $\sim 10^{-4} \text{ A}$) and forward current at low forward voltage. The forward saturation current also shows slight decreasing due to the resistance increment of the TiN/W/Au gate as depicted in Figure 4-13b. Clearly, the Schottky performance had no obvious degradation even by annealing at 800°C for 10 minutes,

indicating the TiN/W/Au gate possessed good thermal stability. It is worth noting that the capacitance also increased when increased the annealing time, implying the change in the metal and AlGaN interface (Figure 4-9b).

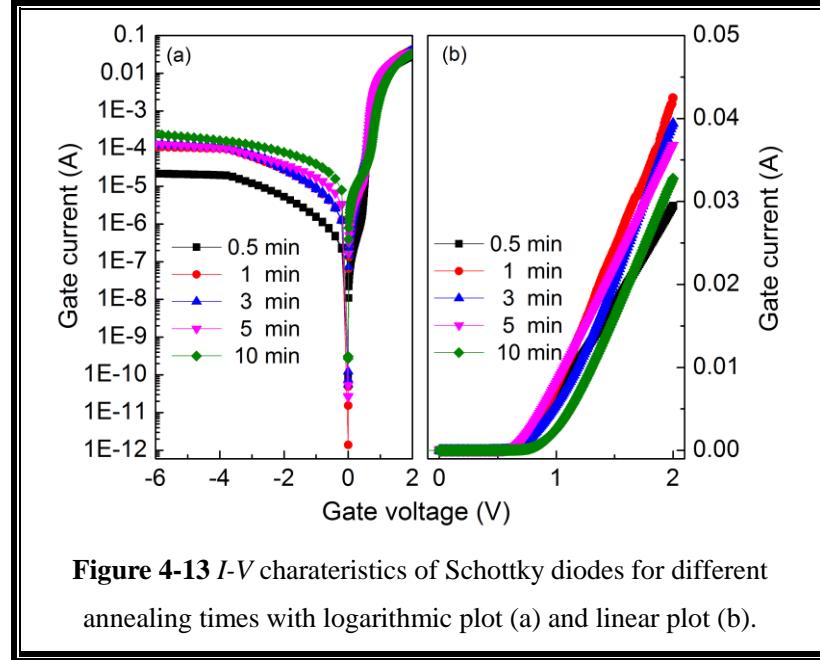


Figure 4-13 *I-V* characteristics of Schottky diodes for different annealing times with logarithmic plot (a) and linear plot (b).

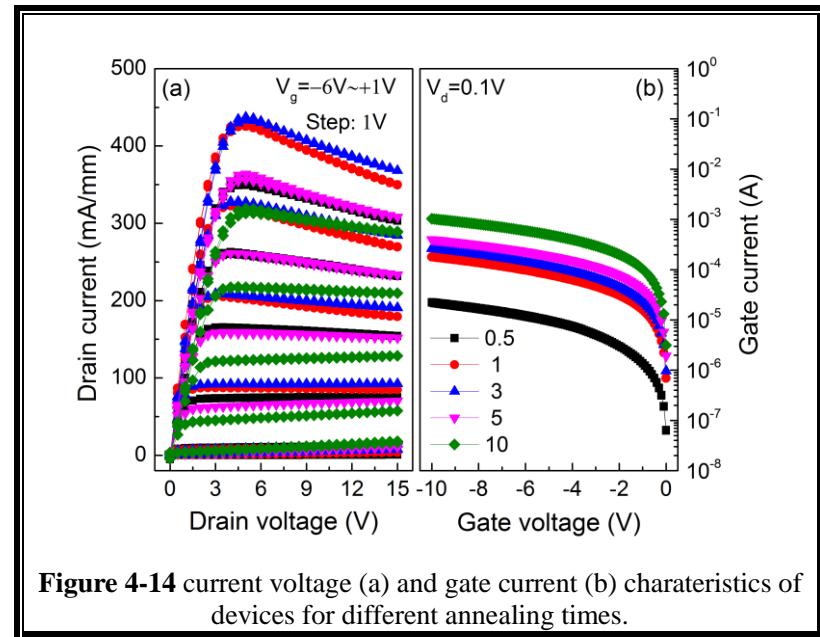
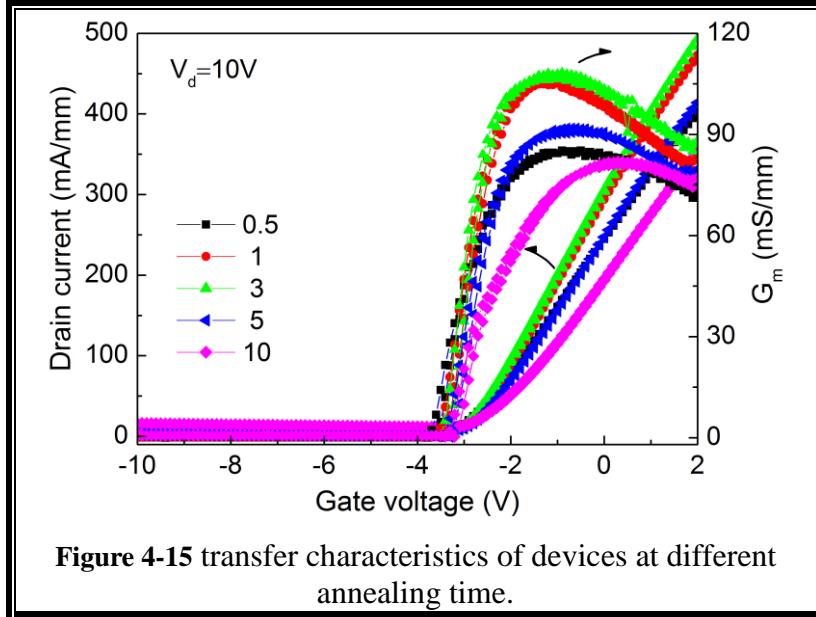


Figure 4-14 current voltage (a) and gate current (b) characteristics of devices for different annealing times.

The annealing time also shows influence on the *I-V* (Figure 4-14) and transconductance (Figure 4-15) characteristics of AlGaN/GaN HFET devices. We found that all the HFETs annealed at different times operated very well with the maximum drain current and transconductance obtained for samples annealed after 1 or

3 minutes. This behavior also related with the resistance variation with annealing time. However, the gate leakage current also increased when annealed at longer time.



§4.3. The fabrication of self-aligned-gate devices

Secondly, TiN-gated devices fabricated by gate-first process were realized. Devices fabricated by a self-aligned gate (SAG) process were then achieved. The flow chart of the process is shown Figure 4-16. Firstly, we optimized the T-gate fabrication process on a silicon substrate using a 3-layer e-beam resist technique.[\[74\]](#) Then, the self-aligned gate HFETs were obtained on AlGaN/GaN wafer with the optimized conditions. For the 3-layer e-beam resist technique, the bottom resist layer was a ZEP520A (500 nm) layer, followed by a LOR 5B (800 nm) resist. The upper layer was also a ZEP520A (500 nm) layer. At the first, the upper layer was exposed by electron-beam and developed. Then, the LOR layer was developed using a specific developer without exposure. Finally, the bottom layer was exposed by electron-beam and developed again. The stack structure of TiN/W/Au (200/50/200 nm) was then deposited to form a T-gate electrode. The drain and source region, including the gate and the access region, were exposed and developed using lithography technology. Ti/Al/Ti/Au multilayers with thickness of 30/120/40/40 nm were formed by lift-off technology for the drain and source contact, where the T-shaped Schottky gate was used as the mask directly. The Schottky gate and the ohmic electrodes were annealed simultaneously at 800 °C for 1 min to obtain ohmic contacts.

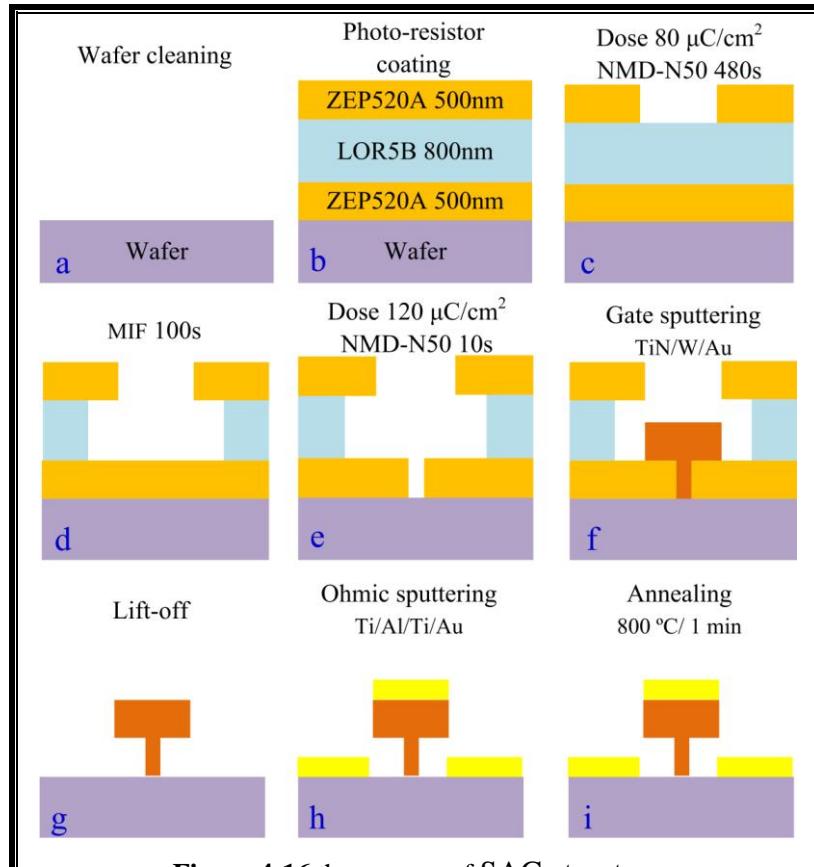


Figure 4-17a is the scanning electron micrograph (SEM) picture of the T-gate on silicon substrate, with a cross-sectional foot width of about 500 nm and a head width of about 2 μm . The AlGaN/GaN HFETs with SAG structure is also shown in Figure 4-17b, with a cross-sectional foot width of about 500 nm and a head width of about 4 μm . The width of the upper layer was enlarged slightly due to the changed conditions on the AlGaN/GaN HFETs substrate.

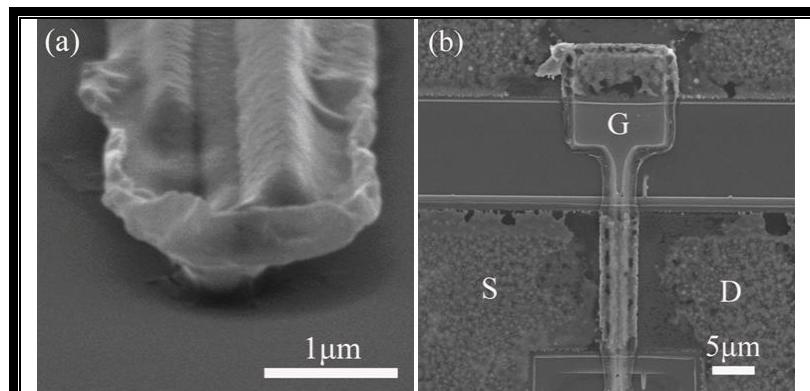


Figure 4-17 the SEM photo of the self-aligned gate device.

The *I-V* characteristics of HFET devices shows that which can operate very well when the gate voltage is swept from -4 to 1 V, with a threshold voltage of -4 V and a maximum drain current density of 540mA/mm (Figure 4-18a). The transconductance (Figure 4-18b) of the obtained device is 130mS/mm. However, there is a hysteresis on the curve and the surface of the electrode after annealing is very rough, more careful optimization is needed to improve the morphology of the device.

Au is believed to prevent the oxidation of the metal surface during the rapid thermal annealing (RTA) process and decrease the total contact resistance. However, the Au diffusion and ball-up can degrade the ohmic contact and surface roughness. Many studies have been conducted to alleviate the disadvantage of Au, such as decreasing the thickness of Au,[75] alternating the diffusion barrier metal,[76] and two and/or multi-step annealing approach.[77] Recently, TiN was also introduced into the ohmic electrode because it can not only prevent the out-diffusion of Ti/Al but also replace Au as the oxidation prevent layer owing to its stability and robust characteristics. [78,79] We are trying to optimize the ohmic electrode with TiN in the future.

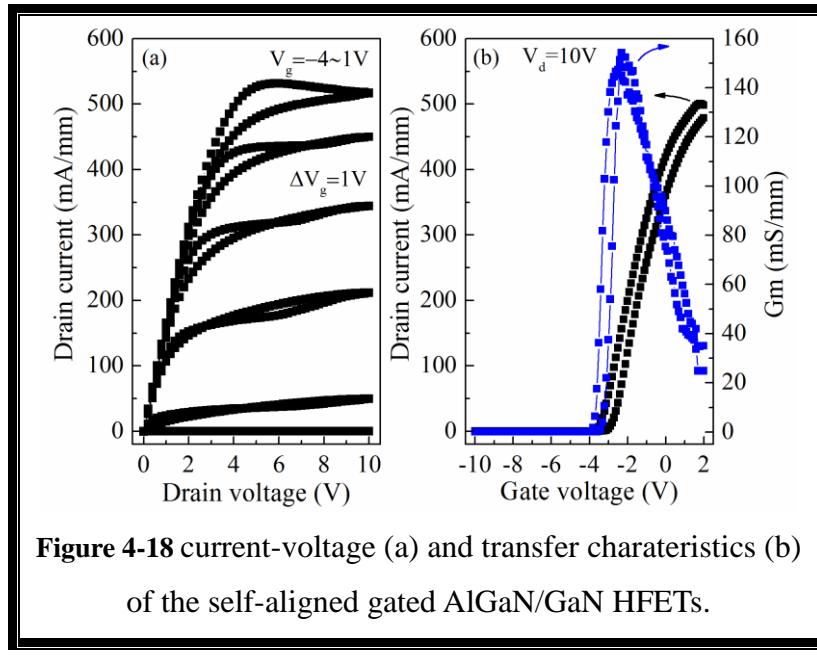


Figure 4-18 current-voltage (a) and transfer characteristics (b)

of the self-aligned gated AlGaN/GaN HFETs.

§4.4. Conclusion

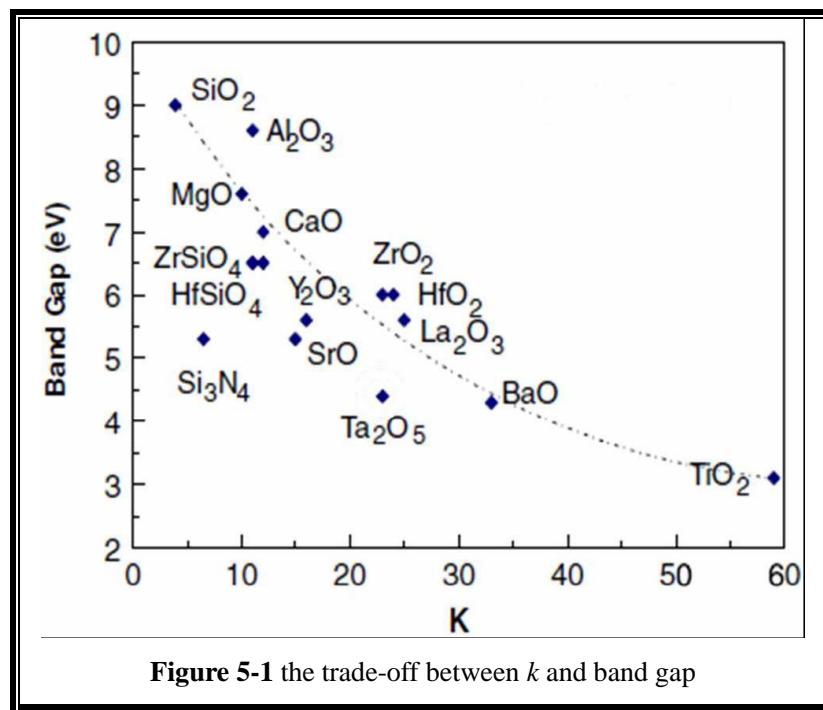
In summary, the effects of annealing temperature and time on the electrical properties of TiN/W/Au-gate AlGaN/GaN HFETs have been investigated. The multilayer of metals could form an ohmic contact when the annealing temperature is higher than 750 °C, and a minimum resistance for annealing at 800 °C for 1 minute

was obtained. On the other hand, the sheet resistance of TiN/W/Au films increased gradually with increasing annealing temperature and time. The high resistance and leakage current were caused by the higher annealing temperature, resulting in the larger on-resistance and smaller drain current. It is demonstrated that annealing at 800 °C for 1 minute results in the lowest on-resistance and highest maximum drain current, while the device performance degraded at higher temperature. Then AlGaN/GaN HFETs with TiN gate were obtained with a self-aligned process, showing a excellent operation with a threshold voltage of about -4 V and a maximum drain current density of 540 mA/mm.

Chapter 5 : Metal-oxide-semiconductor heterostructure field-effect transistors

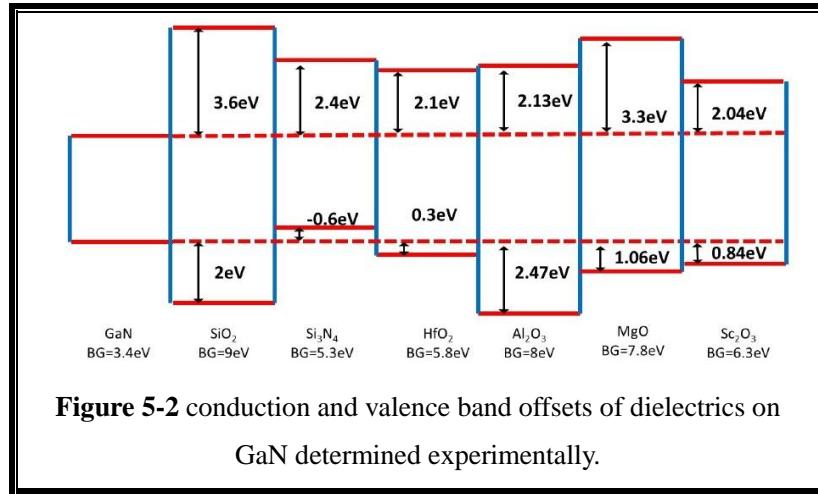
§5.1. The metal-oxide-semiconductor AlGaN/GaN HFETs

In recent years, AlGaN/GaN heterostructure field-effect transistors have been used for high-frequency, high-power and high-temperature applications because of their wide band-gap, high breakdown field and high electron saturation velocity. However, there are two major problems that limit the DC and RF performances of Schottky gate AlGaN/GaN HFETs: 1) serious gate leakage current and 2) RF drain current collapse. These problems lead to the limited gate voltage swing (GVS), increased static power dissipation, reduced breakdown voltage and decreased RF performance. Therefore, AlGaN/GaN HFETs with metal-insulator-semiconductor (MIS) or metal-oxide-semiconductor (MOS) gate structures have been studied. The MOS HFETs design combines the advantages of a MOS structure, which gives a substantially low gate leakage current, and the AlGaN/GaN heterostructure that provides a high density and high mobility 2DEG conducting channel.



According to the International Technology Roadmap for Semiconductors (ITRS)1 Process Integration, Devices, and Structures 2 (PIDS2) table for future high

performance logic technology devices (based on extended planar bulk), an equivalent oxide thickness (EOT) of 6.5 Å is required as early as 2013. The high relative permittivity (high- k) dielectric materials are identified as the most promising candidates for advanced CMOS (complementary metal-oxide semiconductor) devices. Principal requirements for high- k dielectric applications are 1) high dielectric constant 2) high band offset with electrodes (i.e. barrier height) to suppress leakage current 3) thermally and chemically stable in contact with substrate. However, as shown in Figure 5-1, there is a trade-off between the permittivity and band gap, namely, the dielectric materials with a higher permittivity usually show a relative smaller band gap.[80] The band gap can determine the band offset against GaN and a larger band offset is beneficial for obtaining a large barrier height for electron tunneling, as shown in Figure 5-2.[81] Among the available insulator candidates, Al₂O₃, [82] and HfO₂ [83] were commonly used as a gate dielectric and a surface passivation layer. However, HfO₂ dielectric exhibiting low poly-crystallization temperature at about 500 °C[84] and relatively small band-gap than Al₂O₃, Hence, Al₂O₃ is promising due to its high band gap ($E_g=8.8$ eV), a relatively high permittivity (~9) and a large barrier height for electron tunneling (~2.1 eV against GaN).



§5.2. The fabrication of TiN/Al₂O₃/AlGaN/GaN HFETs

Magnetron sputtering technique has the potential of large area, good uniformity, and low-cost to deposit Al₂O₃ thin film at a low deposition temperature. Normally, the Al₂O₃ film deposited by sputtering is amorphous. We did not do the XPS examination due to the limited experimental conditions. However, many reports have presented

that the amorphous Al_2O_3 films are usually with a somewhat lower band gap (~ 6.4 eV) as compared with the bulk material (~ 8.8 eV). T. Hashizume et. al. [85] formed a 3.5 nm Al_2O_3 -based passivation structure by the molecular beam deposition of Al and subsequent ECR- O_2 -plasma oxidation, and the band gap is about 7.0 eV. H. Momida et. al. [86] investigated the structural properties of amorphous Al_2O_3 by first-principles calculations and the band gap of amorphous Al_2O_3 is relatively smaller of about 5.1 to 6.9 eV. Usually, there are two modes of operation that should be considered in reactive sputtering a compound film. [87] Figure 5-3 is a qualitative graph that demonstrates the relationship between the target material (film produced) and the O_2 partial pressure. When the O_2 component is extremely low, both the target and the substrate are mainly covered by pure Al and no Al_2O_3 is deposited on the substrate. Then, within a certain range of O_2 partial pressure, only the substrate is covered by Al_2O_3 while the target is still clean, and the deposition rate begins to drop. This is called the metallic mode. As the O_2 percentage exceeds some critical value, both the target and the substrate are covered by Al_2O_3 finally, which is called poison mode. An abrupt drop of deposition rate occurs at this transition. Note that in general, a higher deposition rate is achieved in the ‘metallic mode’ than in ‘poison mode’. For a fixed total pressure, there is a transition between the poison and metallic modes along with the variation of reactive gas flux, resulting in an obvious hysteresis. In our experiment, the target is pre-sputtered for 10 min with relative higher power and Ar flow rate to remove the residual oxide before deposition.

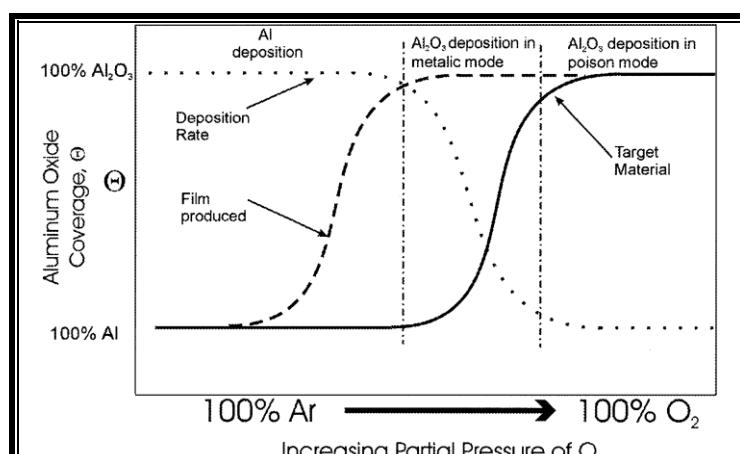


Figure 5-3 growth modes at different partial pressure of O_2 .

Here, we try to fabricate a $\text{TiN}/\text{Al}_2\text{O}_3$ gate stack structure by sputtering

consecutively(Figure 5-4). By this approach, the interface between the oxide layer and the gate metal is improved owing to the sample is kept in vacuum ambient environment. The effects of the oxygen content in the reactive sputtering gas mixture and post annealing temperature upon the device performance was evaluated.

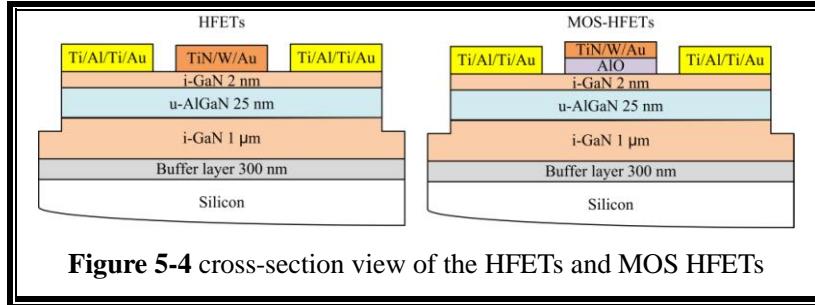


Figure 5-4 cross-section view of the HFETs and MOS HFETs

The epitaxial layers of the AlGaN/GaN HFETs were grown by metal organic chemical vapor deposition on a silicon substrate. The heterostructure consisted of a nucleation layer (about 30 nm thick), a 1 μ m undoped GaN channel layer, a 25 nm undoped AlGaN layer and a 3 nm undoped GaN cap layer from bottom to top. The Al mole fraction of the AlGaN layer was 25%. From the Hall measurement at room temperature, the mobility and average sheet resistance of the two-dimensional electron gas are about $2500 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and $430 \Omega/\square$, respectively.

The device fabrication started with device isolation, which was formed by inductively coupled plasma (ICP) with an etching depth of 100 nm. Ohmic contact metals were then formed using a Ti/Al/Ti/Au (50/200/40/40 nm) multi-layer structure and annealed at 800 °C for 1 min in an N₂ ambient environment. Prior to the gate stack deposition process, the sample surfaces were cleaned by O₂ plasma ashing and immersion in a diluted HCl (HCl:H₂O=1:1) solution for 5 min to remove any oxide layer that developed after the lithography process. An Al₂O₃ layer of about 15 nm nominal thickness was deposited using reactive sputtering in an Ar and O₂ mixture ambient environment with Al target. Finally, the TiN films (about 200 nm) were deposited on Al₂O₃ layer directly in an Ar and N₂ mixture ambient environment (Ar:N₂=15:3) with Ti target. The background vacuum was kept at 2×10^{-5} Pa. Before reactive sputtering, the target was cleaned by sputtering for 10 min in an Ar ambient environment with a power of 150 W. The sputtering power was fixed at 75 W with a chamber pressure of 0.14 Pa during reactive sputtering. The substrate is placed on a water cooling hold over the target with a distance of about 15 cm. To study the effects

of thermal treatment on the MOS structure, three of the samples were annealed at 400 °C for 10 min, 600 °C for 1 min and 700 °C for 1 min, respectively, in rapid thermal annealing (RTA) equipment (N_2 ambient environment). The electrical properties of the devices were evaluated systematically.

§5.2.1. Precursor dependence of the Al_2O_3

To evaluate the effect of the precursor composition, we deposited Al_2O_3 layers using different O_2/Ar reactive sputtering gas ratios (oxygen percentage) of 3:17 (15%), 5:15 (25%), and 10:10 (50%) sccm.

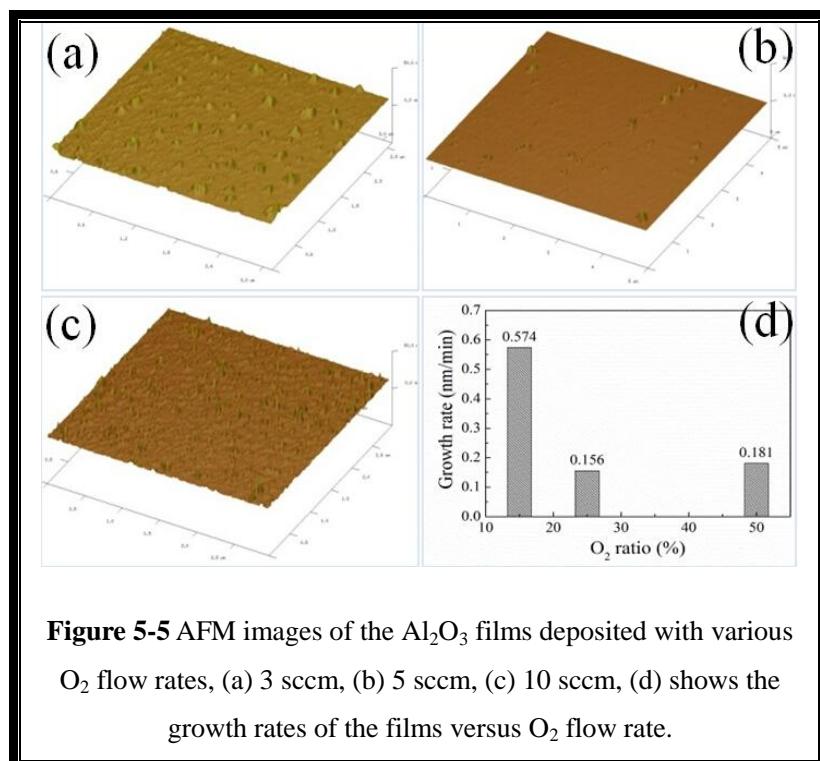


Figure 5-5 AFM images of the Al_2O_3 films deposited with various O_2 flow rates, (a) 3 sccm, (b) 5 sccm, (c) 10 sccm, (d) shows the growth rates of the films versus O_2 flow rate.

The surface morphology of the Al_2O_3 layer is characterized using an atomic force microscope (AFM). When a low O_2/Ar sputtering gas ratio (15%) was introduced, a high density of pyramidal hillocks (PHs) can be observed at the surface of the sample, with a diameter of about 0.2 μm (Figure 5-5a). An obvious decrease in the density was seen for the sample deposited with a medium oxygen sputtering gas content (25%) (Figure 5-5b). Finally, the PHs density increased again when increasing oxygen content in the sputtering gas to 50%. However, the PHs became sharper with a smaller diameter of 0.08 μm (Figure 5-5c). The mechanism responsible for this is considered to be the discrepancy in sputtering rate between each condition. The average

sputtering rates are calculated by dividing the total film thickness by the deposition times. Figure 5-5d shows the sputtering rates versus the O₂/Ar sputtering gas ratios to reveal the effect of precursor composition. It is about 0.574, 0.156, and 0.181 nm/min after adding 15%, 25%, and 40% oxygen, respectively. When the oxygen concentration increased, a decrease of the sputtering yield as well as oxidation of the Al target surface will cause the decrease of sputtering rate that we observe.[88] At a medium O₂ sputtering gas percentage, the lower sputtering rate would cause the number of atoms arriving at the substrate in unit time to decrease. Therefore the atoms absorbed on the substrate surface had enough time to diffuse and react, resulting in a better surface roughness.

C-V characteristic measurements were performed with various frequencies (1KHz~1MHz) by precision LCR Meter. The energy band diagram of an MOS capacitor on a p-type substrate is shown in Figure 5-6. The intrinsic energy level E_i or potential ϕ in the neutral part of device is taken as the zero reference potential. The surface potential ϕ_s is measured from this reference level.

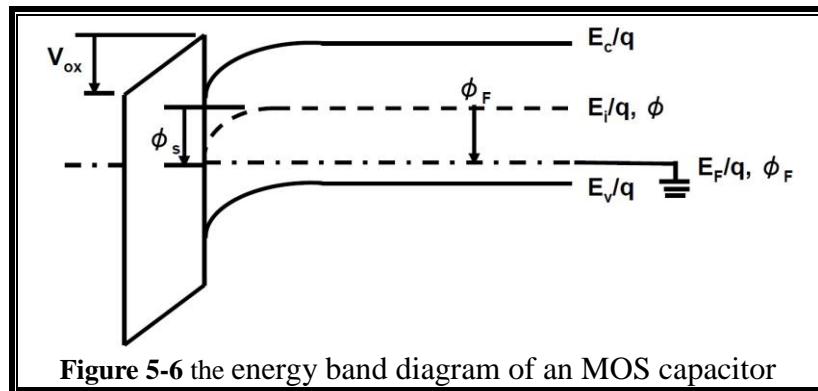


Figure 5-6 the energy band diagram of an MOS capacitor

The capacitance is defined as

$$C = dQ/dV, \quad (5-1)$$

It is the change of charge due to a change of voltage and is most commonly given in units of farad/unit area. During capacitance measurements, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Looking at an MOS-C from the gate, $C = dQ_G/dV_G$, where Q_G and V_G are the gate charge and the gate voltage. Since the total charge in the device must be zero, $Q_G = -(Q_s + Q_u)$ assuming no oxide charge. The gate voltage is partially

dropped across the oxide and partially across the semiconductor. This gives $V_G = V_{FB} + V_{ox} + \phi_s$, where V_{FB} is the flat-band voltage, V_{ox} the oxide voltage, and ϕ_s the surface potential, allowing capacitance to be rewritten as

$$C = -(dQ_s + dQ_{it}) / (dV_{ox} + d\phi_s), \quad (5-2)$$

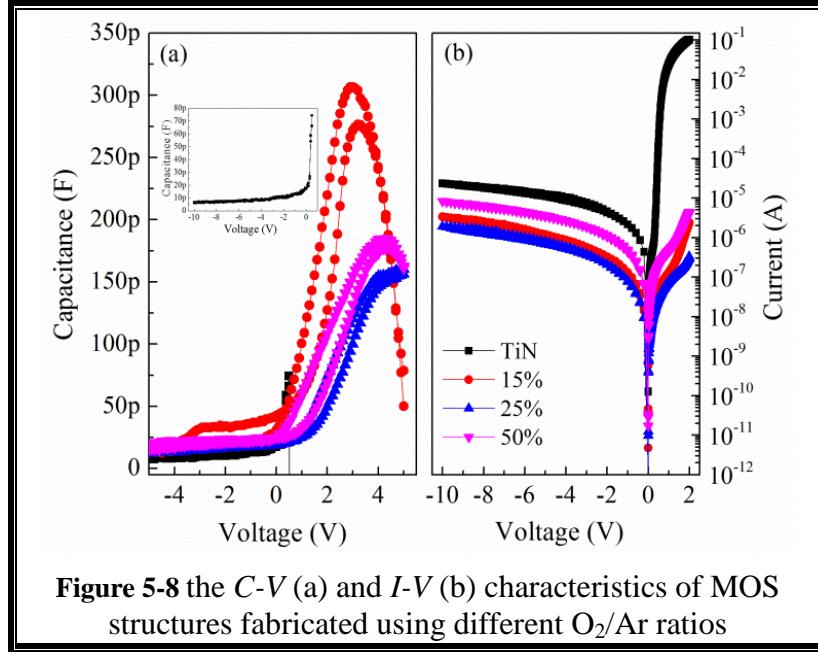
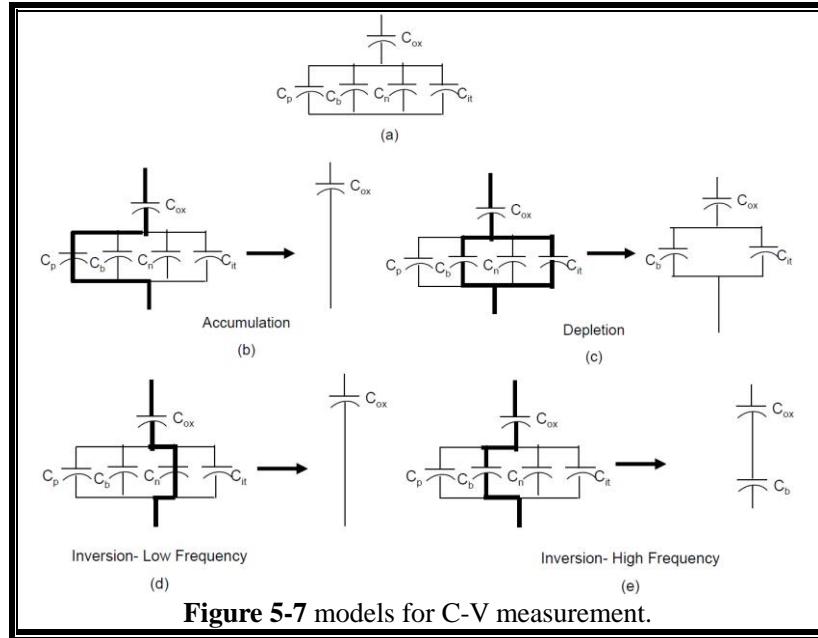
The semiconductor charge density Q_s , consists of hole charge density Q_p , space-charge region bulk charge density Q_b , and electron charge density Q_n . With $Q_s = Q_p + Q_b + Q_{it}$, Eq. (5-2) becomes

$$C = -\frac{1}{\frac{dV_{ox}}{dQ_s + dQ_{it}} + \frac{d\phi_s}{dQ_p + dQ_b + dQ_n + dQ_{it}}} \quad (5-3)$$

Utilizing the general capacitance definition of Eq. (5-1), Eq. (5-3) becomes

$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_p + C_b + C_n + C_{it}}} = \frac{C_{ox}(C_p + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_n + C_{it}} \quad (5-4)$$

The positive accumulation charge Q_p dominates for negative gate voltages for p-substrate devices. For positive V_G , the semiconductor charge are negative. The minus sign in Eq.(5-3) cancels in either case. Equation (5-4) is represented by the equivalent circuit in Figure 5-7(a). For negative gate voltages, the surface is heavily accumulated and Q_p dominates. C_p is very high approaching a short circuit. Hence, the four capacitances are shorted as shown by the heavy line in Figure 5-7(b) and the overall capacitance is C_{ox} . For small positive gate voltages, the surface is depleted and the space-charge region charge density, $Q_b = -qN_A W$, dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of C_{ox} in series with C_b in parallel with C_{it} as shown in Figure 5-7(c). In weak inversion C_n begins to appear. For strong inversion, C_n dominates because Q_n is very high. If Q_n is able to follow the applied ac voltage, the low-frequency equivalent circuit (Figure 5-7(d)) becomes the oxide capacitance again. When the inversion charge is unable to follow the ac voltage, the circuit in Figure 5-7(e) applies in inversion, with $C_b = Ks\epsilon_0/W_{inv}$ with W_{inv} the inversion space-charge region width.



MOS structures were fabricated on Si-doped n-GaN ($1 \times 10^{17} \text{ cm}^{-3}$ dopant density, 1 μm thick) using different O₂/Ar reactive sputtering gas ratios (oxygen percentage) to evaluate the properties. The high frequency (1 MHz) capacitance-voltage (C-V) characteristic of the sample with a pure TiN gate shows a typical Schottky contact curve (inset of Figure 5-8a). The MOS structures obtained at low O₂/Ar ratio possess a big hysteresis with no obvious accumulation regime due to the large forward leakage current. At a medium O₂ sputtering gas percentage (25%), the C-V curve presents clear accumulation and depletion regimes. Meanwhile, the decrease in

hysteresis can be attributed to the reduced interface trap density and the improved trapping behavior of the dielectric. We believe that by introducing oxygen atoms into the film, the oxygen vacancies normally occurred during sputtering were compensated, therefore eliminating the defects and enhancing the film quality. However, the behavior of the dielectric was deteriorated with higher oxygen content in the sputtering gas, which is attributable to the reduction of energy input into the film due to the smaller atomic mass of O than Ar, thus reducing the film density.[89] The corresponding current-voltage (*I-V*) characteristics of circular diodes also showed that the sample with a medium O₂/Ar ratio of 5:15 exhibits the lowest reverse leakage current. To further minimize the remaining hysteresis (interface trap density) in the films, post deposition annealing is an effective approach.

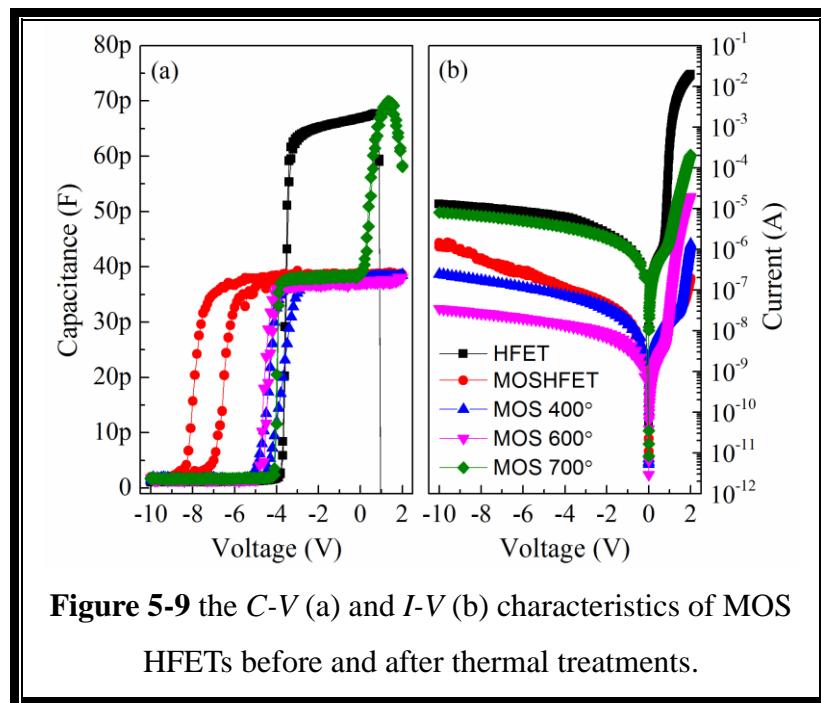


Figure 5-9 the *C-V* (a) and *I-V* (b) characteristics of MOS HFETs before and after thermal treatments.

§5.2.2. Annealing temperature dependence of the Al₂O₃

TiN/Al₂O₃/AlGaN/GaN MOS HFETs were fabricated with a medium O₂/Ar ratio of 5:15, the ratio at which best electric property was achieved in the above experiments, and post annealing at different temperatures to evaluate the annealing temperature dependence of the Al₂O₃ layer. Figure 5-9a shows the high frequency (1 MHz) *C-V* characteristics of circular diodes with a diameter of 166 μm. The *C-V* curves of conventional HFETs show a sharp transition and a negligible hysteresis of about 0.03 V, which demonstrates the high quality interface between TiN and AlGaN.

For the as-deposited MOS HFETs, a slightly stretched curve with an obvious hysteresis (about 1.42 V) is observed, the threshold voltage (V_{th}) observed for HFETs and MOS HFETs are ~3.9 and ~8.0 V, respectively, indicating that an accumulation of positive charge in the oxide is recorded. After thermal treatments, the hysteresis decreases with increasing annealing temperature (about 0.6, 0.25, and 0.03 V for the samples annealed at 400, 600, and 700 °C, respectively.) and the threshold voltage had positive shift. This variation can be attributed to the reduced interfacial state density and the improved trapping behavior of the dielectric inside the oxide and/or at the interface.[90] However, the threshold voltage positively shifted closing to the HFETs and the capacitance at the positive bias increased sharply after 700 °C annealing. One possible reason is the crystallization of Al_2O_3 when the sample was annealed at 700 °C. More recently, evidence of the formation of microcrystalline structures has been confirmed by transmission electron microscopy (TEM) for ALD- Al_2O_3 annealed at 700 °C in N_2 for 1 min. If this occurs, the electron can transport through the oxide layer due to the linkage of the grain boundaries to form a leakage current path.[91] Another possible reason is the titanium diffusion into the Al_2O_3 film, because the reactively-sputtered TiN film is a Ti-rich film. This is also consistent with the reverse leakage current which increased sharply after 700 °C annealing (Figure 5-9b). Assuming the same sheet charge density in the channel for MOSHFET and HFET devices at zero gate bias and ignoring the surface charge Q_s at the dielectric/AlGaN interface, the threshold voltages for the MOSHFET and HFET can be related as:

$$Q_s = qN_s = C_{MOSHFET} \times V_{TMOS} = C_{HFET} \times V_{THFET} \quad (5-5)$$

$$V_{TMOS} = C_{HFET} \times V_{THFET} / C_{MOSHFET} = V_{THFET} \times \left(1 + \frac{d_{ox} \times \epsilon_b}{d_b \times \epsilon_{ox}} \right) \quad (5-6)$$

Here $C_{MOSHFET}$ and C_{HFET} are the capacitances of equal area pads on the oxide and non-oxide areas and ϵ_{ox} is the dielectric permittivity of the gate dielectric; d_{ox} and d_b are the thicknesses of dielectric and barrier layers correspondingly, V_{TMOS} and V_{THFET} are correspondingly the absolute values of the MOSHFET and HFET threshold voltages.

While for the V_{TMOS} model take the charge into account,[92] we assume piezoelectric charges P at the III-N heterostructure interfaces, barrier surface donors $N_{d,surf}$, oxide/barrier interface traps charge N_{it} , and bulk and interfacial defect oxide

charge. Defect charges within the III-N heterostructure layers are assumed to be negligible compare to large polarization charges at the interfaces. On the other hand, fixed (i.e., independent of V_g) oxide charge has to be taken into account as it can strongly differ for different oxides. Depending on the location, interfacial $N_{ox,intf}$ (formed from the oxide/GaN interface a few monolayers onwards) and bulk $N_{ox,bulk}$ (uniformly distributed across the oxide bulk) oxide charges are assumed. V_{TMOS} can be then expressed as:

$$V_{TMOS} = \phi_b - \Delta E_C - \phi_F - \frac{d_{ox}}{\epsilon_{ox}} P_1 - \frac{d_{ox} \times \epsilon_{cap} + d_{cap} \times \epsilon_{ox}}{\epsilon_{cap} \times \epsilon_{ox}} P_2 - \frac{d_{ox} \times \epsilon_{cap} \times \epsilon_b + d_{cap} \times \epsilon_{ox} \times \epsilon_b + d_b \times \epsilon_{ox} \times \epsilon_{cap}}{\epsilon_{cap} \times \epsilon_{ox} \times \epsilon_b} P_3 - \frac{d_{ox} \times q}{\epsilon_{ox}} \left(N_{d,surf} + N_{it} + N_{ox,intf} + \frac{d_{ox}}{2} N_{ox,bulk} \right) \quad (5-7)$$

where ϕ_b is the metal barrier height for TiN/Al₂O₃, ΔE_C is the conduction band discontinuity for Al₂O₃/GaN interface, ϕ_F is the energy difference between the E_C and Fermi energy E_F , d is the thickness, ϵ is the permittivity, and the subscripts ox , cap , and b refer to the oxide, GaN cap, and AlGaN barrier layer, respectively. P_1 , P_2 , and P_3 are the total polarization sheet charges (given by a sum of spontaneous and piezoelectric polarization) at the GaN-cap surface, GaN-cap/AlGaN interface, and AlGaN/GaN buffer interface, respectively

Theoretically, the threshold voltages of our MOSHFET when ignoring the surface charge is about -6.8 V, which is positive than the measured value, indicating that an accumulation of positive charge in the oxide is recorded. After thermal treatments, the hysteresis decreases with the increase of the annealing temperature and the threshold voltage become close to the HFETs. It can be attributed to the reduced interfacial state density and the improved trapping behavior of the dielectric inside the oxide and/or at the interface. The remained slightly V_{TMOS} shift towards negative side is due to the increased gate to channel separation after the insert of insulating layer. However, the capacitance at a positive bias of the sample after 700°C anneal is close to the HFETs, this may be caused by the crystallization that annealing at a higher temperature. More recently, evidence of the formation of microcrystalline structures

has been confirmed by transmission electron microscopy (TEM) for ALD-Al₂O₃ annealed at 700°C in N₂ for 1 min. If this occurs, the electron can transport through the oxide layer due to the linkage of the grain boundaries to form a leakage current path.

The permittivity of the alumina can be estimated by using the following equation:

$$\frac{1}{C_{MOSHEMT}} = \frac{1}{C_{HEMT}} + \frac{1}{C_{oxide}} \quad (5-8)$$

where $C_{MOS-HEMT}=38$ pF and $C_{HEMT}=66$ pF is the zero-bias capacitance, $C_{oxide} = \frac{\epsilon_0 \epsilon_{oxide} S}{d_{oxide}}$, ϵ_0 is vacuum permittivity, $S=2.16\times10^{-4}$ cm² is the capacitor area. The estimated oxide permittivity is about 7 with the nominal thickness (d_{ox}) of 15 nm, which is small than the theory value of 9. This is probably due to real oxide thickness is higher than the nominal thickness. The gate leakage of the MOSHFETs (Figure 5-9b) also shows an anneal temperature dependence. It initially decreased from $\sim 10^{-5}$ to $\sim 10^{-8}$ with the temperature increased to 600 °C, which can be attributed to the decrease of interface trap assisted tunneling. While annealed at 700 °C, the crystalline of the oxide will caused the increase of the leakage current.

§5.2.3. The leakage mechanism of the Al₂O₃

Among electrical characteristics, the carrier conduction mechanism in the insulator was worthy enough to be measured. Typically, two possible mechanisms are explored in the metal-insulator interface: Schottky emission and Frenkel-Poole emission.[93] The Schottky-Richardson emission, generated by the thermionic effect, is caused by electron transport across the potential energy barrier via field-assisted lowering at a metal-insulator interface. The leakage current equation is as follows:

$$J = A^* T^2 \exp\left(\frac{\beta_s \sqrt{E} - q\Phi_s}{kT}\right), \beta_s = \sqrt{\frac{q^3}{4\pi\epsilon\epsilon_0}}, \quad (5-9)$$

Where A^* is the effective Richardson constant, and Φ_s is the contact potential barrier. The $\ln J \sim \sqrt{E}$ plots should be a line:

$$\ln J = \frac{\beta_s}{kT} \sqrt{E} + \left[\ln(A^* T^2) - \frac{q\Phi_s}{kT} \right]. \quad (5-10)$$

The Frenkel-Poole emission refers to electric-field-enhanced thermal emission

from a trap state into a continuum of electronic states-usually, but not necessarily, the conduction band in an insulator (Figure 5-10). The current density associated with Frenkel-Poole emission is given by: [94-96]

$$J = C_0 E \exp\left(\frac{\beta_{FP} \sqrt{E} - q\Phi_{FP}}{kT}\right), \beta_{FP} = \sqrt{\frac{q^3}{\pi\epsilon\epsilon_0}}, \quad (5-11)$$

Where E is the electric field in the semiconductor barrier at the metal-semiconductor interface, Φ_{FP} is the barrier height for electron emission from the trap state, ϵ is the relative dielectric permittivity at high frequency, T is temperature, ϵ_0 is the permittivity of free space, and k is Boltzmann's constant. Because the electrons emitted from the trap states do not polarize the surrounding atoms, the relevant dielectric constant is that at high frequency, rather than the static dielectric constant. From Eq.5-11, we can find that the current transport by Frenkel-Poole emission, the $\ln(J/E)$ should be a linear function of \sqrt{E} ,

$$\ln(J/E) = \frac{\beta_{FP}}{kT} \sqrt{E} + \left[\ln C_0 - \frac{q\Phi_{FP}}{kT} \right]. \quad (5-12)$$

The leakage current mechanism in MOSHFETs after 600 °C annealing was analyzed by temperature dependent current-voltage measurements (Figure 5-11). When the temperature is below 200K, the leakage current is nearly independent of temperature, indicating that the conduction is dominated by tunneling transport. There is a valley came out at a voltage and shift to about 0V with the increase of temperature, this may be attributed to the transient process of the interfacial state trapping. For temperatures above 200 K, the measured macroscopic current is observed to be dependent on both gate voltage and temperature. Specifically, we observe the reverse-bias leakage current of the MOSHFETs structure a linear dependence of $\ln(J/E) \sim \sqrt{E}$, it is possible for that the Frenkel-Poole emission, which refers to electric field enhanced thermal emission from a trap state into a continuum of electronic states-usually, but not necessarily, the conduction band in an insulator, can correctly describes current transport at higher temperatures.

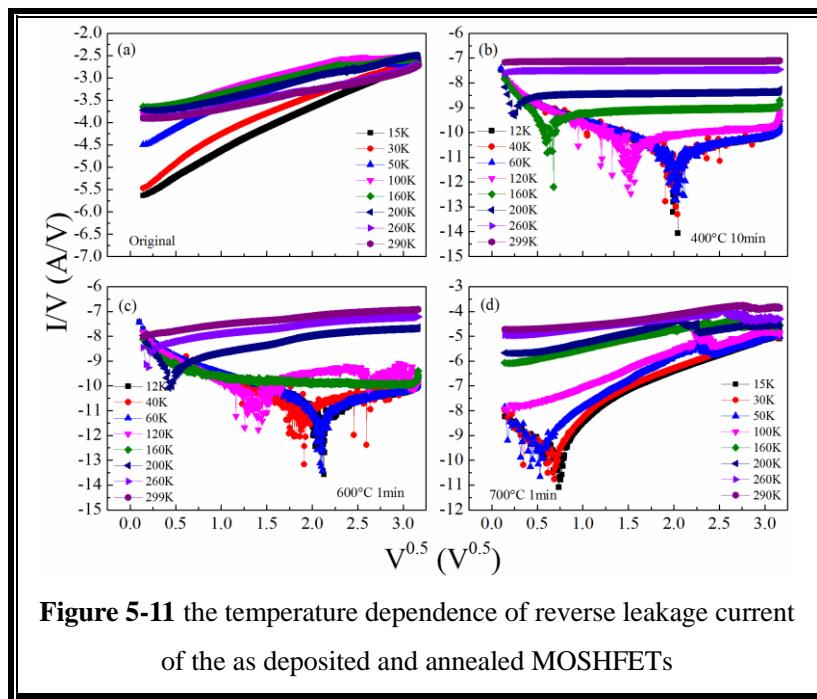
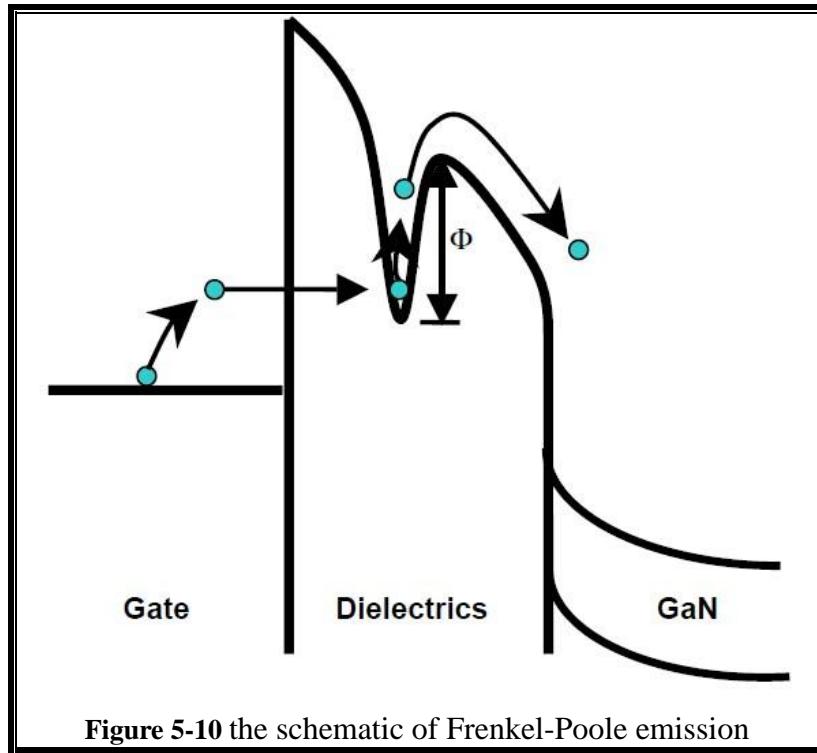


Figure 5-12a shows the I - V characteristics of the conventional and MOSHFETs devices with a gate length and a gate-source/drain spacing of 3 and 3 μm , respectively. The gate voltage is swept from -6 to 0 V. Both of the devices are operate well. For the HFETs, a decrease in drain current at a higher drain-source voltage is due to self-heating and the decreased electron mobility. For the MOSHFETs annealed at

600°C, though the threshold voltage is close to HFETs, the maximum drain current is much smaller than the conventional device, owing to the smaller transconductance (Figure 5-12b).

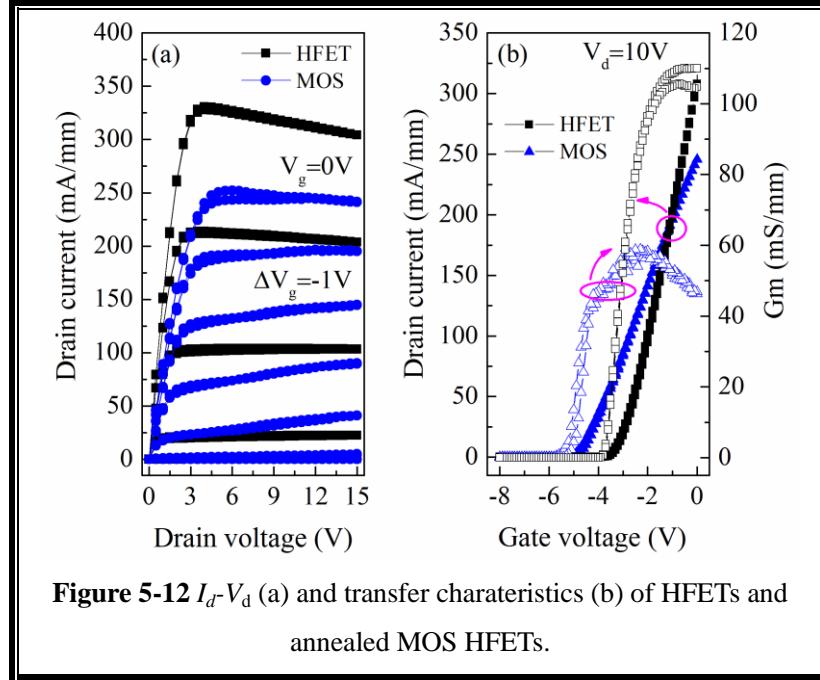


Figure 5-12 I_d - V_d (a) and transfer characteristics (b) of HFETs and annealed MOS HFETs.

g_m is a figure-of-merit value that measures the effectiveness of the gate in modulating the drain current. In the saturation region of a transistor, it can be defined as:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) \quad (5-13)$$

where μ is the carrier mobility, W is the gate width, L is the gate length, and C_{ox} is the gate oxide capacitance per unit area:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad (5-14)$$

Therefore, a larger oxide thickness reduces the gate capacitance, which in turn, reduces g_m . Another important parameter in determining the transistor performance is the unity-current gain cutoff frequency (f_T), which can be derived from the small-signal model as:

$$f_T = \frac{g_m}{2\pi(C_{GS} - C_{GD})} \quad (5-15)$$

where C_{GS} and C_{GD} are the capacitances between gate and source/drain. Thus, the g_m degradation due to the additional Al_2O_3 reduces the switching speed of the MOSHFETs.

§5.3. The fabrication of TiN/HfON/AlGaN/GaN HFETs

As discussed above, although the TiN/ Al_2O_3 gate stack could improve the interface performance and decrease the gate leakage from $\sim 10^{-5}$ to $\sim 10^{-8}$ after annealing, but at the expense of a significant decrease in device transconductance and a large negative shift in threshold voltage owing to the further separation between the gate metal and the semiconductor layer. If we can improve the poly-crystallization temperature of HfO_2 , it may be another dielectric candidate.

Hafnium oxynitride (HfON) has a higher crystallization temperature(800 °C) than pure HfO_2 (500 °C), a large band gap (6.7eV), and reasonable conduction band offset to GaN. It was reported that HfON film formed by incorporating N into HfO_2 could acts as a crystallization inhibitor, distort the equilibrium of the lattice, produce disordered states, improve the thermal stability and electrical properties of these gate dielectric films, because of the existence of Hf-N bonds in the bulk as well as the existence of N at the dielectric/GaN interface. [97,98] HfON films have been reported to have a crystallization temperatures up to 800-950 °C, and their amorphous structure as well as the Hf-N bonding are effective in blocking oxygen diffusion.[99] However, the nitrogen incorporation in HfON is not stable thermally. [100] Annealing leads to O substitution for N. Furthermore, nitrogen incorporation will lead to the increase of the fixed charges at the interface, the decrease of band gap and band offset, and degrade the electrical properties. Therefore, nitrogen concentration (N/O atomic ratio), should be carefully controlled to guarantee excellent properties of HfON high-k dielectrics as oxygen exhibits a stronger reactivity than nitrogen with regard to the metal.[101] It is worth further studying on the electrical and material characterization of HfON film.

Here, we try to fabricate a TiN/HfON gate stack structure by sputtering consecutively. Base on the results of the Al_2O_3 deposition, we choose a medium O_2/Ar ratio of 5:15 to obtain the HfO_2 film. By adding nitrogen in the O_2/Ar mixture, we can obtain the HfON film. The effects of the nitrogen content in the reactive sputtering gas mixture upon the device performance was evaluated.

§5.3.1. Precursor dependence of the HfON

To evaluate the effect of the precursor composition, we deposited HfON films on sapphire substrates using different nitrogen flow rates (O_2/Ar gas ratio is 5:15) of 0, 1, 5, and 10 sccm. The surface morphology and the growth rate of the HfON films are characterized using an atomic force microscope (AFM). When only a O_2/Ar sputtering gas was introduced, HfO₂ film was obtained with a growth rate of 0.75 nm/min and showed a high density of round liked particles at the surface of the sample (Figure 5-13). When the nitrogen flow rate was 1 sccm, the growth rate decreased slightly while the morphology is similar with the sample obtained without nitrogen. The size of the particles became uneven when 5 sccm nitrogen was introduced and some particles with obvious larger diameter can be observed in the film. Finally, the film in the sputtering gas with 10 sccm nitrogen showed a smallest growth rate of about 0.57 nm/min and the surface morphology was unlike all the other samples. When the nitrogen concentration increased, a further decrease of the sputtering yield as well as nitride of the Hf target surface will cause the decrease of sputtering rate that we observe. With 10 sccm nitrogen, the lowest sputtering rate cause the number of atoms arriving at the substrate in unit time to decrease. Therefore the atoms absorbed on the substrate surface had enough time to diffuse and react, resulting in a better surface roughness.

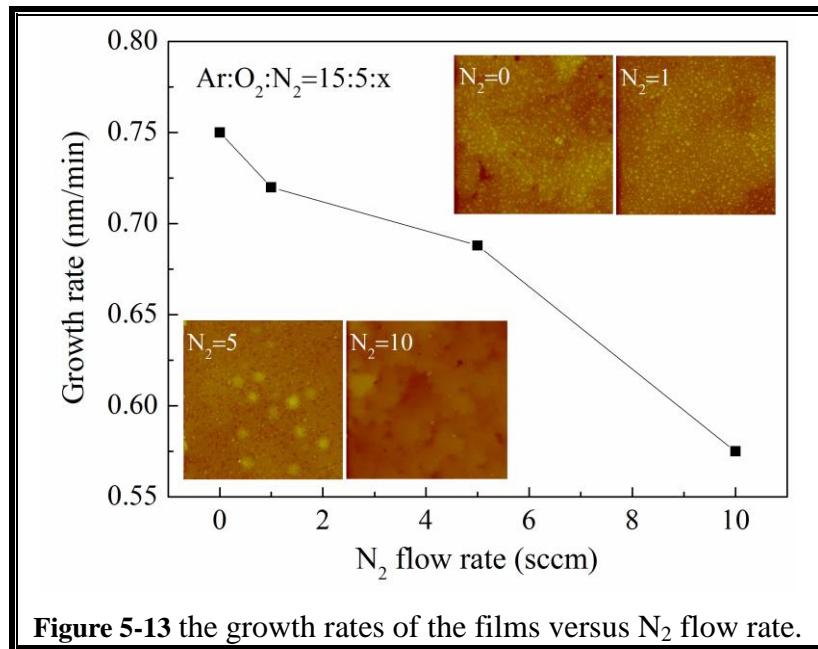


Figure 5-13 the growth rates of the films versus N₂ flow rate.

MOS structures were fabricated on Si-doped n-GaN ($1 \times 10^{17} \text{ cm}^{-3}$ dopant density, 1 μm thick) using different N₂ reactive sputtering gas (nitrogen percentage) to

evaluate the properties. The high frequency (1 MHz) capacitance-voltage (Figure 5-14) characteristic of the sample with a TiN/HfO₂ film gate presents clear accumulation and depletion regimes. The corresponding *C-V* curves of the capacitor with HfON film nitride by 1 sccm nitrogen, the flat-band voltage is shifted to a more negative value in comparison with non-nitride films, indicating a formation of positive charges. By scanning dc bias back and forth during *C-V* measurements, this capacitor with the non-nitrided film shows no obvious hysteresis. While for the film nitride by 5 sccm nitrogen, the curve was stretched with an obvious hysteresis that can be attributed to the increase of interface trap density and the deterioration of trapping behavior of the dielectric. Finally, when the nitrogen flow rate increased to 10 sccm, the capacitance of the MOS structures shows no variation with the voltage.

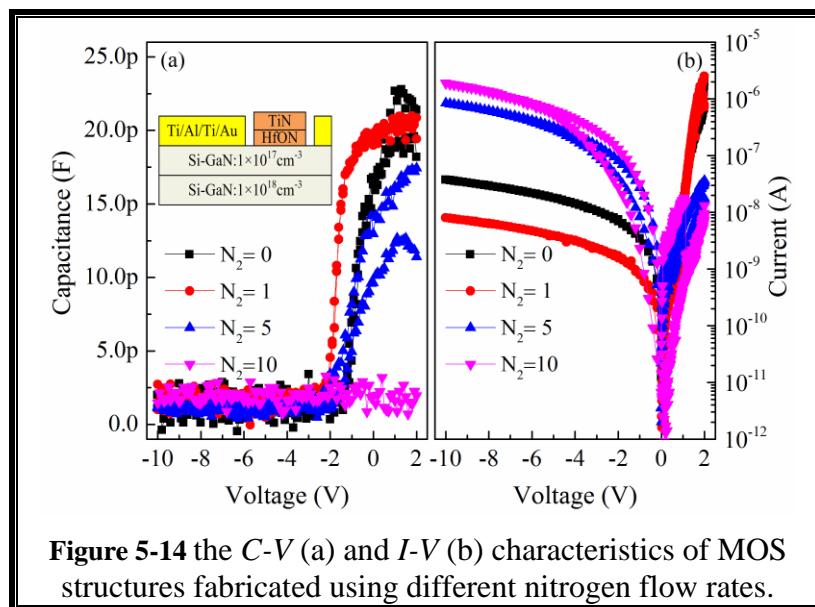


Figure 5-14 the *C-V* (a) and *I-V* (b) characteristics of MOS structures fabricated using different nitrogen flow rates.

The bonding status of the films was evaluated by XPS. Figure 5-15 is a typical normalized spectra of HfON films deposited with different N₂ flow rates. After sputtered for 180s, the Hf-4f spectrum of the sample deposited without nitrogen can be fitted with two peaks which can be attributed to HfO₂ (Hf-4f^{7/2}: 16.5 eV, Hf-4f^{5/2}: 18.2 eV). It was also reported that the Hf-4f^{7/2} peak at 17.3 eV, separated by 1.6 eV from the Hf-4f^{5/2} peak at 18.9 eV, originates from Hf bounded to oxygen.[102] When 1 sccm nitrogen was introduced into the precursor, the spectrum of the sample is similar with the nitrogen free one. While further increased the nitrogen flow rate increased to 5 sccm, the spectrum can be fitted into three peaks at about 15.9 eV, 17.4

eV and 20.8 eV. The new came out peak at about 20.1 eV dominated the spectrum of the sample deposited with 10 sccm nitrogen. Usually, the binding energy observed in the XPS at a higher nitrogen concentration should shift to lower energy.[103] However, in the N-1s spectra, only noise signal can be detected from the samples without and with lower nitrogen in the reactive ambient. While a relatively obvious peak centered at about 398 eV can be observed with the nitrogen flow rates of 10 sccm, indicating the nitride of the film. Therefore, the origination of this new come out peak is not clear and may be related to some Hf-O-N mix material. In the O-1s core level spectra, the major peaks appear around 530 eV, which can be assigned to the lattice oxygen of HfO_2 . The peak in the O-1s spectra also shift to about 533 eV, which can be assigned to the hafnium oxynitride. The Hf-4f spectra, as well as the O-1s spectra, indicating a gradually transformation from hafnium oxide to hafnium oxynitride due to the higher nitrogen in the reactive gases.

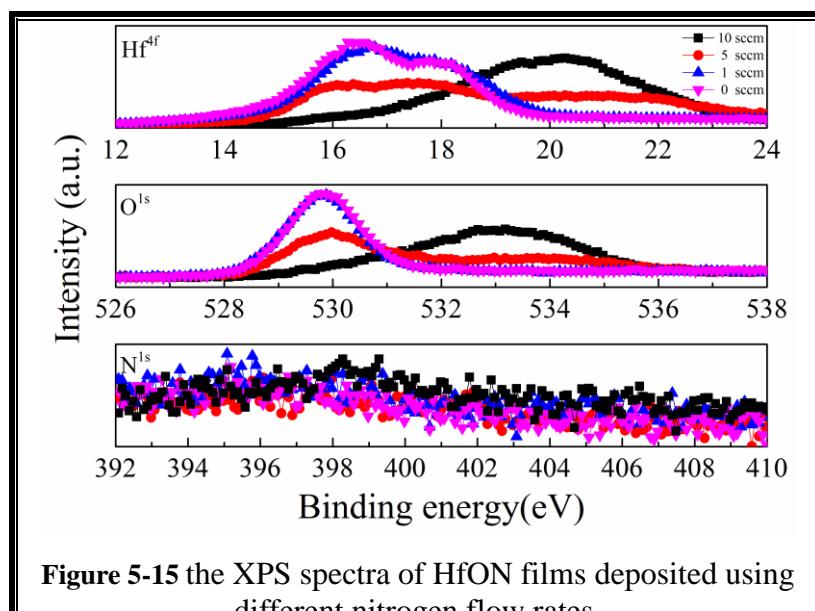
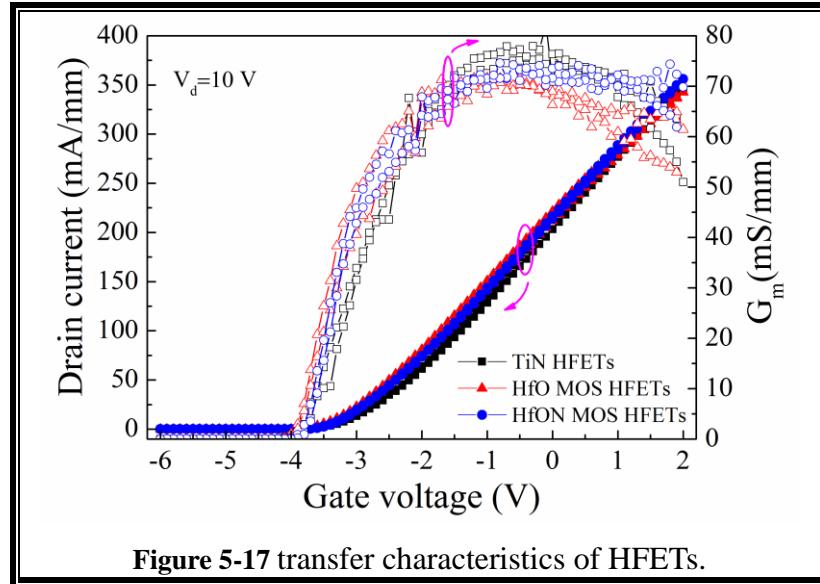
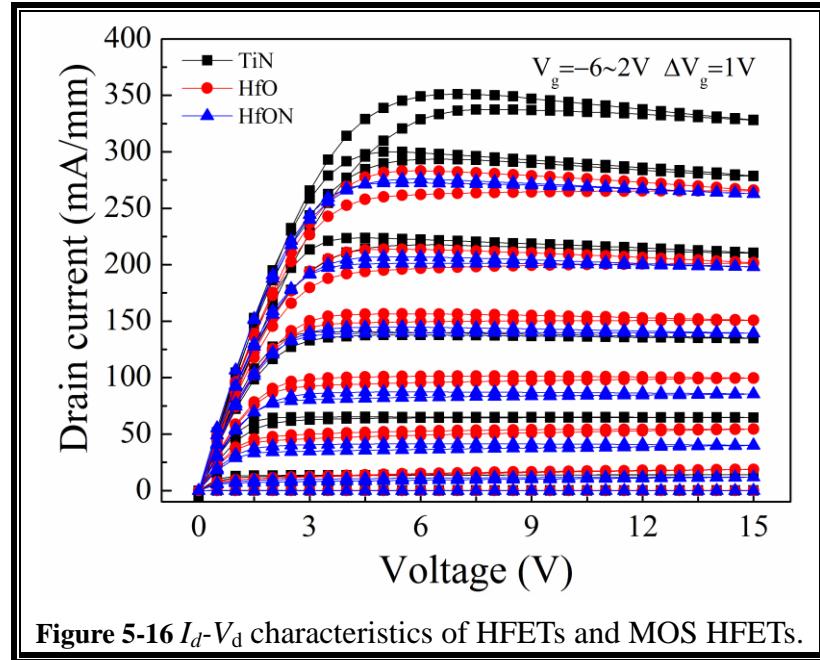


Figure 5-15 the XPS spectra of HfON films deposited using different nitrogen flow rates.

§5.3.2. The characteristics of the TiN/HfON/AlGaN/GaN HFETs

Figure 5-16 shows the $I-V$ characteristics of the TiN-gated and MOSHFETs devices with a gate length and a gate-source/drain spacing of 3 and 3 μm , respectively. The gate voltage is swept from -6 to 2 V. All of the devices can operate well with the saturation current exhibiting a negative conductance at large drain voltage. The decrease in drain current at higher drain-source voltage is due to the self-heating and the decreased electron mobility. There is an obvious hysteresis in the curve of

TiN-gated HFETs and it is slightly decreased after the introducing of HfO_2 dielectric, which can be attributed to the decrease of interface trap density in the dielectric. While the devices with HfON show no obvious hysteresis, indicating the nitridation is an effective way to decrease of interface trap density. For the HfON MOS HFETs, the maximum drain current is only slightly smaller than that of TiN-gated HFETs.



Unlike with the Al_2O_3 MOSHFETs, the threshold voltages and the transconductance of the HfO_2 and HfON MOSHFETs are comparable to that of TiN-gated HFETs (Figure 5-17). The higher permittivity of the HfO_2 and HfON than

the Al_2O_3 results in the improving of transconductance of the MOSHFETs devices. Even without thermal treatments, the hysteresis is very weak and the threshold voltage is close to the HFETs, which can be attributed to the lower interfacial state density and the improved trapping behavior of the Hf-based dielectric inside the oxide and/or at the interface.

The corresponding gate current-voltage (I_g - V_g) characteristics of bar-type device also showed that the TiN-gated HFETs possessed good rectification characterization with a reverse leakage current of about 10^{-8} A (Figure 5-18). Introducing of the HfO_2 and HfON dielectric resulted in the decrease of both reverse leakage current and forward current. As compared with the HFETs, the reverse leakage current of the HfON MOSHFETs is about two order lower due to the decrease of defect density which assists the carrier tunneling.

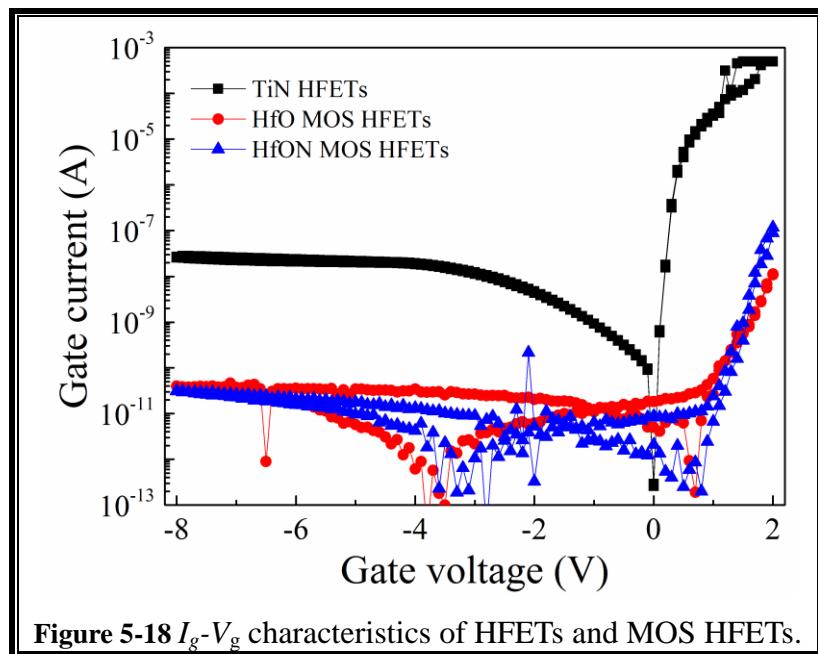


Figure 5-18 I_g - V_g characteristics of HFETs and MOS HFETs.

§5.4. Conclusion

Several TiN/ Al_2O_3 /GaN metal-oxide-semiconductor structures are deposited using different O_2/Ar reactive sputtering gas ratios and are post annealed at different temperatures. The Al_2O_3 films deposited with the medium oxygen content show the best behavior of dielectric. The result of post deposition annealing on the device performance showed that the MOS structure annealed at 600°C for 1 min possessed a smaller hysteresis and reverse leakage current. The reduction of effective oxide charge and total interface trap density had contributed to the reduction of leakage

current density of the annealed oxides. With annealing, the maximum transconductance shows slightly decreased, resulting in the decrease of saturate drain current.

The high-k nitrogen doping HfO_2 dielectric was also deposited using reactive sputtering. We found that the growth rate, surface morphology, and composition were gradually transformed from hafnium oxide to hafnium oxynitride by adding the nitrogen into the reactive gases. The MOS capacitor fabricated with HfON film nitride by 1 sccm nitrogen shows the smallest reverse leakage current in the I - V characteristic and presents clear accumulation and depletion regimes in the C - V characteristic. As compared with the TiN-gated HFETs, the threshold voltage of the HfON MOSHFETs shows no obvious shift while has a slightly smaller transconductance, resulting in the relatively lower drain current. Beside of this, the leakage current is obviously decreased by the introducing of the HfON dielectric.

Chapter 6: Conclusions and Future Works

§6.1. Summary and Conclusions

Over the past three decades, AlGaN/GaN heterostructure field-effect transistors (HFETs) has become a very promising candidate for the next generation high voltage and high power electronic devices, mainly due to the superior material properties of GaN. To achieve a high-temperature performance, it is very desirable to produce gate contacts with a large Schottky barrier height (SBH) and excellent thermal stability. In high-frequency applications, it is beneficial to minimize the access resistances and reverse leakage current. This thesis has sought to propose and experimentally realize various technology options to solve the challenges faced by the AlGaN/GaN HEMTs.

Firstly, we choose the refractory metal nitrides as Schottky contact candidate on GaN. The results demonstrate that TiN possess good rectification, good adhesion strength, and excellent thermal stability after thermal treatment at 850°C for 1 min. For further study, several TiN films are deposited using different N₂/Ar reactive/inert sputtering gas ratios, thereby varying the nitrogen content present in the sputtering gas. Films deposited with a medium (40% and 60%) nitrogen content show the best film quality and thermal stability. The Schottky diodes with reactively sputtered TiN electrodes have a lower turn-on voltage compared with the diodes with Ni electrode, while the on-resistance, the reverse leakage current and the reverse breakdown characteristics are comparable to each other. Therefore, the TiN electrode is suitable for application in the high-temperature AlGaN/GaN HFETs.

Furthermore, we try to accomplish the self-aligned-gate (SAG) process to minimize the access resistances by reducing the spacing among the electrodes. We evaluated the annealing temperature and time-dependent electrical properties of AlGaN/GaN HFETs utilizing TiN/W/Au as the gate electrode to obtain the best annealing condition for the ohmic contact, which also shows lowest affect on the gate electrode. These results demonstrated that the TiN/W/Au gate, which can withstand 800 °C annealing for a short time, is suitable for application in the self-aligned-gate process for AlGaN/GaN HFETs. Base on those results, AlGaN/GaN HFETs with TiN gate were obtained with a self-aligned process, showing a excellent operation with a threshold voltage of about -4 V and a maximum drain current density of 540 mA/mm.

Finally, metal-oxide-semiconductor structure deposited using reactive

sputtering were introduced to minimize the reverse leakage current. The Al₂O₃ films deposited using a medium O₂/Ar reactive sputtering gas ratios and post annealing at 600°C for 1 min possessed a smaller hysteresis and reverse leakage current. However, the maximum transconductance shows slightly decreased, resulting in the decrease of saturate drain current. The high-k nitrogen doping HfO₂ dielectric was then deposited using reactive sputtering to alternate the Al₂O₃. The MOS capacitor fabricated with HfON film nitride by 1 sccm nitrogen shows obviously decreasing reverse leakage current and presents good C-V characteristic. As compared with the TiN-gated HFETs, the threshold voltage of the HfON MOSHFETs shows no obvious shift while has a slightly smaller transconductance, resulting in the relatively lower drain current. Beside of this, the leakage current is obviously decreased by the introducing of the HfON dielectric.

§6.2. Suggestion for future works

As shown in chapter 3, by alternated the Ni electrode with reactively-sputtered TiN, the GaN Schottky barrier diodes (SBDs) with low turn-on voltage are developed for microwave rectification. The diodes with reactively-sputtered TiN electrodes have a lower turn-on voltage compared with the diodes with Ni electrode, while the on-resistance, the reverse leakage current and the reverse breakdown characteristics are comparable to each other. However, the reverse leakage current is also an important factor in the application of rectenna circuit. New Schottky material with a balance between the turn-on voltage and the reverse leakage current is desirable.

The MOSHFETs can effectively decrease the reverse leakage current of the devices. However, the crystallization that caused by annealing at a higher temperature of about 700°C results in the transport of electron through the oxide layer due to the linkage of the grain boundaries to form a leakage current path. Then, the oxide film is not suitable for application in the self-aligned-gate process, which usually need a 800°C annealing. Raising the crystallization temperature or decreasing the ohmic annealing temperature is necessary.

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Biography

Liuan Li was born in Hengyang, Hunan province, China on 7th April 1986.

2003.09-2007.07: he graduated with a Bachelor of Science degree in physics from Jilin University, China.

2007.09-2010.07: he was recommended to complete his Master of Science degree in condensed matter physics from State Key Laboratory of Superhard Materials, Jilin University, China.

2010.09-2012.04: he served as a failure analysis engineer in SAE magnetic Ltd., a subsidiary of the TDK corporation.

2012.04-present: he has been engaged in the investigation of high-frequency and high-power AlGaN/GaN field effect transistors in The University of Tokushima, Tokushima, Japan.

He has received the following awards:

The Koraku Award of Miki education foundation (平成 26 年度康樂賞)

The Research Award of International Exchange, The University of Tokushima (平成 26 年度国際交流研究奨励賞).

The Education and Research Assisting Award of Faculty of Engineering, The University of Tokushima (平成 26 年度徳島大学工学部教育研究助成奨学賞).

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