

## 論文内容要旨

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| 報告番号  | 甲 先 第 <b>230</b> 号   | 氏 名 | 王 青 鵬 |
| 学位論文題目  | Development of enhancement-mode GaN MOSFET on AlGaIn/GaN heterostructure<br>(AlGaIn/GaNヘテロ構造上エンハンスメント型GaN MOSFETの開発) |     |       |
| 内容要旨  |  |     |       |
| <p>Compared with Silicon, GaN has great potential on the application of low power consumption devices for its wide bandgap of 3.4 eV. GaN MOSFETs have become one of the most attractive research areas. In my thesis, there are four parts will be introduced, they are 1) device and process design of GaN MOSFET on AlGaIn/GaN heterostructure; 2) study of the accurate mobility and interface state density characterization method of GaN MOSFET; 3) process optimization for GaN MOSFETs on AlGaIn/GaN heterostructure; and 4) device and process design of gate-first GaN MOSFET, self-aligned GaN MOSFETs and GaN HEMTs.</p> <p>In chapter 2, several possible structures of GaN MOSFETs are given an elaborate comparison and analysis. Device design of GaN MOSFET on AlGaIn/GaN heterostructure is elaborately illustrated including the layout design and fabrication process design. In the end of this chapter, some preliminary experiments on the dry recess process are done including the etching gas flow rate, etching protection mask and the etching chamber pressure. Atomic force microscope (AFM) was used to investigate the etching profile, surface roughness etc. It is found that the etched surface would be with higher gas flow rate will show higher roughness with granular hillock with height of more than 20 nm. PR masked samples show stronger trenching effect and rougher surface. Also, suspected deposition effect is found in the condition of higher chamber pressure which is not beneficial to obtain a clean GaN surface. Finally, a relatively optimum dry recess condition with SiO<sub>2</sub> etching protection mask, etching gas flow of 3 sccm, etching chamber pressure of 0.25 pa was confirmed.</p> <p>In chapter 3, the problems in characterization of GaN MOSFETs were analyzed based on our experiments. It is found that even in the same sample, the extracted channel mobility will be quite different with different device pattern when using the traditional <math>C-G_m</math> method. A phenomenon of parallel channel caused by worse field isolation at the gate pad outside the channel was found in bar-type GaN MOSFETs based on AlGaIn/GaN heterostructure. It will result a phenomenon of two-piece mobility and finally lead an overestimation on the mobility extracted by the <math>C-G_m</math> method. Also, the variation of channel length extracted by electrical measurement was found. It will lead an obvious underestimation on mobility, especially</p> |  |     |       |

in the case of short channel MOSFETs. To characterize the channel mobility precisely, we have verified and analyzed these phenomena and presented several improved methods to characterize the mobility of MOSFETs. The mobility of  $130 \text{ cm}^2/\text{Vs}$  extracted by our method agreed quite well with that extracted from a long channel ring type MOSFET which was thought to be reasonable showing these methods are effective to obtain the correct value of the channel mobility. In the end of this chapter, the interface state density extraction method was given a brief introduction on both I-V method of MOSFET and C-V method of MOS capacitor.

In chapter 4, process optimization including the etching gas, etching bias power, etching protection mask, oxide type, oxide thickness of the GaN MOSFETs are investigated and analyzed. The charges near the  $\text{SiO}_2/\text{GaN}$  interface of the GaN MOSFETs with different etching conditions were evaluated. It is found that stronger bombard damages in dry process will bring more charges near the interface and finally make the threshold voltage of the device becoming more negative. The effects of nitrogen plasma treatment and ammonia water treatment were investigated. These treatments are effective and can recover or remove the dry etching damaged layer. An E-mode GaN MOSFET with the maximum field-effect mobility of  $148.12 \text{ cm}^2/\text{Vs}$  was realized by ammonia water treatment. GaN MOS capacitors were also prepared to investigate the influence of these treatments on the interface state densities using Terman method. The corresponding interface state density for the ammonia water treated sample was around  $3 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$  in the  $E_c-E_t$  range from 0.2 to 0.6 eV.

In chapter 5, Low temperature ohmic process was developed on both SI-GaN, n-GaN and AlGaIn. Gate-first GaN MOSFET, self-aligned GaN MOSFET and AlGaIn/GaN HEMT were fabricated using the low temperature ohmic formation process assisted by ICP dry etching system. Based on common lithography technology, a narrow access space of  $0.3\text{-}0.5 \text{ }\mu\text{m}$  between schottky and ohmic electrodes was realized. Based on a ICP dry-etching assisted room temperature ohmic process, the gate-first GaN MOSFET with maximum channel mobility of  $163.8 \text{ cm}^2/\text{Vs}$  was realized. With  $500 \text{ }^\circ\text{C}$   $\text{N}_2$  annealing, ohmic contact on the ICP treated region and schottky contact on the untreated region were realized at the same time on AlGaIn or SI-GaN. The self-aligned devices show good pinch-off characteristics. The maximum output current and transconductance were  $393 \text{ mA/mm}$  and  $100 \text{ mA/mm}$  for the self-aligned HEMT and MOSFET, respectively. The easier fabrication process made these devices very practical in fabrication of self-aligned devices.

## 論文審査の結果の要旨

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| 学位論文題目<br>Development of enhancement-mode GaN MOSFET on AlGaN/GaN heterostructure<br>(AlGaN/GaNヘテロ構造上エンハンスメント型 GaN MOSFETの開発)  |   |     |                      |
| 審査結果の要旨<br><p>本研究はAlGaN/GaNヘテロ構造上にエンハンスメント型 GaN MOSFETを実現するため、デバイス構造と試作工程の設計、試作プロセスの最適化、デバイス評価の研究、デバイス性能の向上を目的にした。</p> <p>まず、AlGaN/GaNヘテロ構造上に GaN MOSFET を実現するため、デバイス構造、プロセス工程、マスクを設計した。完成したデバイスを AFM で観察し、デバイス特性を評価しながら、リセスプロセスとしての ICP ドライエッチング条件を最適化した。次に、GaN MOSFET を正確に評価するため、デバイスモデルから評価パターンを提案し、設計した。この方法を用い、完成したデバイスを測定し、評価方法を確立した。さらに、ICP ドライエッチングガスとバイアス、エッチング保護膜、酸化膜の種類と厚さなどのリセスプロセス条件の移動度、界面準位、しきい値電圧などのデバイス特性への影響について、詳しく調べた。ICP ドライエッチングダメージにより、デバイスのしきい値電圧は負になることが判った。また、窒素プラズマ、アンモニア水で表面処理によりダメージの回復や除去する実験も試した。最後に、ICP ドライエッチングダメージを利用し、GaN デバイスの低温オーミックプロセスを開発した。室温や 500 °C で N<sub>2</sub> 中アニールにより、SI-GaN, n-GaN と AlGaN/GaN ヘテロ構造上にオーミック特性が得られた。その低温オーミックプロセスを利用し、ゲート先 GaN MOSFET やセルフアラインゲート GaN MOSFET 及び AlGaN/GaN HEMT を試作し、優れたデバイス特性を得た。</p> <p>以上本研究は、AlGaN/GaNヘテロ構造上にエンハンスメント型 GaN MOSFETに関する研究であり、本論文は博士（工学）の学位授与に値するものと判定する。</p> |   |     |                      |