様式８

論　文　内　容　要　旨

報告番号	甲　先　第　303　号	氏　名	石　文
学位論文題目	High performance intra algorithm and parallel hardware architecture for the next generation video coding 次世代動画像符号化標準における高効率画面内予測アルゴリズム及びそのアーキテクチャに関する研究		

内容要旨

As the next generation video coding standard, HEVC supports higher resolution video coding and achieves about 50¥% bit-rate reduction under the same visual quality compared with Advanced Video Coding. In HEVC, intra coding reduces data redundancy in neighboring blocks, which leads to high data dependency and high-power consumption. The targets of the research are to reduce the computational complexity, increase coding performance and realize hardware parallelization.

Three novel schemes are proposed to realize the above-mentioned targets. Firstly, an edge detector based fast level decision algorithm for intra prediction of HEVC is presented to reduce the redundant calculation and encoding time. The proposed algorithm utilizes the high correlation between regional texture and prediction unit partitioning. It is mainly composed of a bottom-up level decision method and an efficient decision flow based on an authentic image feature. Furthermore, chrominance information is also employed to decide the prediction unit partitioning. Secondly, an adaptive downsampling signal based intra prediction for parallel intra coding of high efficiency video coding is proposed to improve coding efficiency and reduce data dependency. Downsampling signal is applied to generate prediction samples instead of neighboring pixels. It reduces spatial redundancy and removes the data dependency in intra encoding for coding tree unit (CTU) structure. Meanwhile, a fast training method is designed to derive downsampling signal adaptively. Thirdly, hardware implementation oriented fast intra coding based on downsampling information for HEVC is presented to realize parallel hardware implementation for real-time applications. The scheme is consisted of two parts, preprocessing stage and fast intra coding stage. Three downsampling information based fast decision algorithms are proposed in fast intra coding stage. Moreover, a parallelized architecture of the fast intra coding scheme is presented. The preprocessed downsampling stage can be executed with intra coding stage in parallel.