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論　文　内　容　要　旨

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学位論文題目	Built-in Quiescent Supply Current Test Circuits for Electrical Interconnect Tests in 3D Stacked ICs (3D積層ICの静的電源電流による電気的配線テストのための組み込み型検査回路に関する研究)		

内容要旨

3D stacked ICs using Through-Silicon Vias (TSVs) have gained a lot of interest among semiconductor industry as an excellent alternative to cope with some challenges faced in system-on-chips (SoCs). A 3D stacked IC is fabricated by stacking multiple known good dies (KGDs) and vertically connected with TSVs and micro bumps. This enables interconnects between KGDs in 3D stacked IC to be shortened, and the small area footprint can be achieved. In addition, it can realize a high speed operation and low power dissipation.

Open defects may occur at interconnects between KGDs and at input/output pins in an IC during fabrication processes of TSVs and also during stacking processes of KGDs. In this paper, the open defects are classified into the following three types: hard open defects, resistive open ones and capacitive open ones. They are the ones to be detected in this paper.

In order to realize high reliability of manufactured 3D stacked ICs, it is indispensable to test interconnects between dies in them. Since the open defects can cause electrical discontinuity in circuits made of the ICs, the above three types of open defects must be detected to guarantee sufficient outgoing product quality to the customers. Thus, interconnect tests of 3D stacked ICs are vital in order to detect open defects occurring at interconnects between KGDs.

In this paper, two kinds of electrical interconnect test methods and built-in test circuits have been proposed to detect open defects occurring at interconnects between dies and input/output pins in 3D stacked ICs. Both of the electrical interconnect test methods are based on quiescent supply current that is made to flow through an interconnect under test. The open defects are detected by measuring voltages caused by the supply current and by comparing them to a pre-specified threshold value.

Boundary scan flip flops implemented in dies are utilized in the first proposed electrical test method. The built-in test circuit is made of an nMOS and a diode that are added to each input interconnect of each die. Testability of the test method is evaluated by SPICE simulations and experiments of a PCB circuit made of a prototyping IC embedding the test circuit. The simulation results reveal that an open defect generating additional delay time of 279psec and an open defect that generates no logical errors, are detected by the test method at a test speed of 200MHz. The open defects inserted to the PCB circuit are also detected by the

test method at a test speed at least of 1MHz. Furthermore, the testability is compared to an electrical test method with a built-in test circuit made of only an nMOS. It is concluded that resistive open defects of smaller resistance are detected with the test circuit made of an nMOS and a diode.

In the second proposed electrical test method, boundary scan flip flops are not utilized in tests. A new built-in test circuit has been proposed for the test method. The built-in test circuit is composed of a pair of nMOS and pMOS switches which are added to each input interconnect of each die. The testability is evaluated by SPICE simulations and by some experiments of a PCB circuit made of a prototyping IC embedding the test circuit. Open defects that are inserted to the PCB circuit in the experiments are detected by the test method at a test speed of 500kHz. The simulation results show that resistive open defects of 150Ω and above, and a capacitive open defect, which generates no logical errors with a minimum crack height of 37nm, are detected by the test method at a test speed of 1MHz.