Doctoral Thesis

Built-in Quiescent Supply Current Test Circuits for Electrical Interconnect Tests in 3D Stacked ICs

(3D 積層 IC の静的電源電流による電気的配線テストのための組み込み型検査回路に関する研究)

College of System Innovation Engineering

Graduate School of Advanced Technology and Science

Tokushima University

FARA ASHIKIN BINTI ALI

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Abstract

The semiconductor industry has become increasingly interested in three-dimensional stacked integrated circuits (3D stacked ICs) using through-silicon vias (TSVs) as an alternative to cope with challenges faced in system on chips (SoCs). They are fabricated by stacking multiple known good dies (KGDs) with TSVs and microbumps. In a 3D stacked IC, stacking shortens interconnects between KGDs and enables a small footprint; they can also achieve a high operation speed and low power dissipation.

Open defects can occur at interconnects between KGDs in an IC during fabrication of the TSVs and stacking of the KGDs. This paper identifies three classifications for open defects: hard, resistive, and capacitive open defects. Testing interconnects between dies is indispensable to producing high reliability in manufactured 3D stacked ICs. Because open defects can cause electrical discontinuity in circuits made of ICs, the three types of open defects must be detected to guarantee a sufficient outgoing product quality level to customers. Interconnect tests of 3D stacked ICs are therefore vital to detect open defects occurring at interconnects between KGDs.

In this paper, two kinds of built-in test circuits and electrical interconnect test methods are proposed to detect open defects at interconnects between dies in 3D stacked ICs. Both of the electrical interconnect test methods are based on a quiescent supply current that is made to flow through the interconnect under test. Open defects are detected by measuring voltages caused by the supply current and comparing them to a pre-specified threshold value.

Boundary scan flip flops implemented in dies are used in the electrical test method with one built-in test circuit. The test circuit is made of nMOSs, and diodes are added to each input interconnect of each die. The test method is evaluated using SPICE simulations and experiments with a PCB circuit made of a prototype IC containing the test circuit. The simulation results reveal that both an open defect-generating additional delay time of 279 psec and an open defect that generates no logical errors are detected by the test method at a test speed of 200 MHz. Open

defects inserted into the PCB circuit are also detected by the test method at a test speed of 1 MHz. The testability is comparable to an electrical test method using a built-in test circuit made only of nMOSs. Resistive open defects of smaller resistance are detected with the proposed test circuit made of nMOSs and diodes than the defects detected with a circuit made only of nMOSs.

The other built-in test circuit is for testing 3D stacked ICs made of dies in which boundary scan flip flops are not embedded. A test circuit and a test method are proposed to detect open defects in the ICs. The built-in test circuit is composed of a pair of nMOS and pMOS switches that are added to each input interconnect of each die. The testability is evaluated by SPICE simulations and by experiments using a PCB circuit made of a prototype IC containing the test circuit. Open defects inserted into the PCB circuit in the experiments are detected by the test method at a test speed of 500 kHz. The simulation results show that open defects with resistance of 150 Ω and above and the open defects generating no logical errors are detected by the test method at a test speed of 1 MHz.

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Chapter 1 Introduction

The semiconductor industry has continuously pursued size reduction, high-density integration, cost reduction, and low power consumption in a wide range of markets, including industrial, home electronics, and mobile devices. Over the past 40 years, progress in IC technology has been guided by Moore's law, which states that IC density will double every two years, as shown in Figure 1.1, in which the number of transistors per chip is plotted against years [1]. Now, systems on chips (SoCs) must confront the limitations of chip density [2, 3].

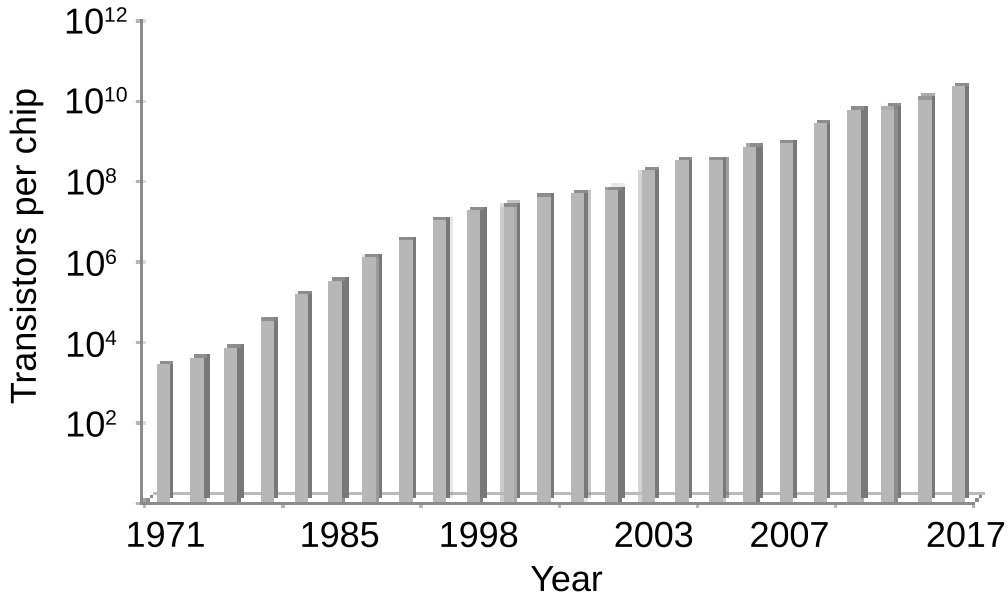


Figure 1.1 A plot of transistors per chip against year [1]

Three-dimensional stacked integrated circuits (3D stacked ICs) have recently been brought to the industry's attention [4]; in a 3D stacked IC, interconnects between logic gates in dies are shortened by stacking them, achieving a smaller footprint area and realizing high operation speeds [5]. Wires in a microprocessor consume more than 30% of the power [6]; as the total length of wires between gates is shortened by stacking dies, ICs can achieve lower power dissipation [7, 8]. Stacking dies allows ICs to achieve both low power dissipation and high operation speeds [9].

In realizing a 3D stacked IC, several 3D interconnect technologies have been proposed with binding wires, through-silicon vias (TSVs), and contactless interconnection [10]. TSVs offer the potential for the greatest interconnect density of these three options. As a result, 3D stacked ICs using TSVs have been extensively explored and drawn much interest in the semiconductor industry [11]. This paper discusses how to test 3D stacked IC made of TSVs and microbumps.

A typical configuration for a 3D stacked IC is shown in Figure 1.2. The ICs are fabricated by stacking known good dies (KGDs) with microbumps in an IC package [5, 7]. KGDs are made by forming TSVs inside dies vertically to connect to a silicon layer in another die. TSVs are effective connections due to their capacity for high-speed operation [5].

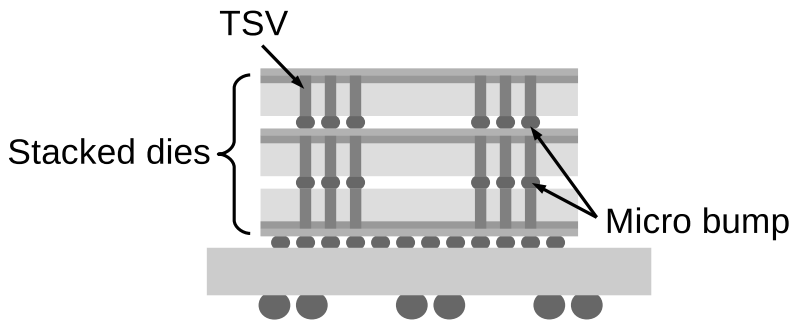


Figure 1.2 Schematic diagram of 3D stacked IC

Despite their benefits, there are challenges to realizing a high yield of 3D stacked ICs using TSVs. Significant issues include the volatile processes during TSV and KGD stack fabrication, as well as the aging process caused by electromigration and stress migration [8], [12] - [14]. In these processes, short and open defects can occur at interconnects between KGDs. The aging process can also lead to the occurrence of short and open defects at interconnects between dies inside the ICs, which ultimately cause malfunctions. Thus, interconnect tests between dies in the ICs before shipment to market are essential to guarantee sufficient outgoing product quality to customers.

Generally, interconnect testing of 3D stacked ICs can be classified into two types: pre-bond and post-bond testing [15]. Pre-bond testing is conducted on dies before stacking to select KGDs. Post-bond testing is conducted after KDGs are stacked.

Defects can occur at interconnects between KGDs during the stacking process, so only post-bond testing is discussed in this paper.

Interconnects between dies in 3D stacked ICs can be tested by a logical test, the boundary scan test method [5]. A boundary scan test circuit of IEEE 1149.1 standard is embedded in many dies for 3D stacked ICs. Short defects between two interconnects will cause logical errors by providing complement logic signals to the boundary scan test circuit. This means that short defects are easy to detect using the boundary scan test method [5], but this method method can be time-consuming because there are a huge number of interconnects in 3D stacked ICs. To reduce the test time, various kinds of design-for-testability (DfT) methods and built-in test circuits have been proposed [16] - [21].

Open defects occurring at interconnects between dies in 3D stacked ICs are more difficult to detect than short ones, because it is not apparent what faulty effects are caused by such defects. Since open defects at interconnects between dies are difficult to detect, they are the only ones considered in this paper.

This paper classifies open defects into the following three types: resistive, capacitive, and hard open defects. Resistive open defects can be caused by a void or crack at an interconnect; even when a void or a crack occurs at an interconnect, the parts to be connected remain connected to each other electrically with a resistor. For a capacitive open defect, an interconnect is completely separated into two parts that are not connected to each other, but if the gap between the two parts is short, logic signals will be propagated through the gap. For hard open defects, the gap between the two parts is long enough so a logic signal cannot be propagated to the other part.

This paper discusses how to detect and locate these three kinds of open defects. Two kinds of built-in electrical interconnect test circuits and test methods are proposed and evaluated by SPICE simulations and experiments. One of the test circuits uses boundary scan flip flops embedded in dies to provide test input vectors. This allows interconnects between dies with embedded flip flops to be tested. The other test circuit does not use flip flops, so 3D stacked ICs made of dies without flip flops can also be tested.

This paper is organized as follows: the fabrication processes for 3D stacked ICs and the defects occurring at interconnects between KGDs are introduced in Chapter 2, along with defects occurring in the field due to aging processes. Chapter 3 summarizes the proposed interconnect test methods for detecting defects occurring at interconnects between dies in 3D stacked ICs. In Chapter 4, the built-in test circuit and electrical interconnect test method for 3D stacked ICs made of dies containing boundary scan flip flops are described, together with the evaluation results. In Chapter 5, the proposed test method for 3D stacked IC without embedded flip flops is described, along with the results of the testability analysis. The conclusions of this paper are presented in Chapter 6.

Chapter 2 Defects at Interconnects in 3D stacked ICs

This chapter introduces the manufacturing processes for 3D stacked ICs and the defects at interconnects that can occur during these processes before discussing built-in test circuits. Defects can also occur after 3D stacked ICs are shipped to market; such defects are caused by aging in the ICs, and the causes are introduced in this chapter.

2.1 Defects in Stacking Processes

The stacking process consists of TSV formation and the stacking of KGDs. The defects occurring in these processes are introduced in this section.

2.1.1 Defects in TSV Formation Processes

TSVs are fabricated inside dies before stacking. Figure 2.1 illustrates the typical fabrication flow of TSVs in a wafer [22].

The fabrication of TSVs starts with the etching of via holes inside the die to be stacked at Step (1) in Figure 2.1. This can be done by the deep reactive-ion etching (DRIE) method in a BOSCH process, a high-aspect ratio plasma etching process that alternates a short step of SF_6 plasma. This allows the isotropic removal of silicon with short C_4F_8 plasma deposition to create a protection layer at the sidewall [60].

After the etching process, the deposition of a silicon dioxide (SiO_2) layer used as an insulator inside the via holes is conducted at Step (2) to isolate TSVs from the surrounding silicon substrate electrically. This is followed by the fabrication of a barrier layer onto the SiO_2 layer. Both of the layers can be deposited using the plasma-enhanced chemical vapor deposition (PECVD) technique.

After the deposition of the SiO_2 and barrier layers, a copper seed layer is sputtered onto the structure, followed by filling copper into the vias in an electroplating process at Step (3) in Figure 2.1. Next, chemical-mechanical planarization (CMP)

is used to remove overburden copper and smooth the wafer surface at Step (4).

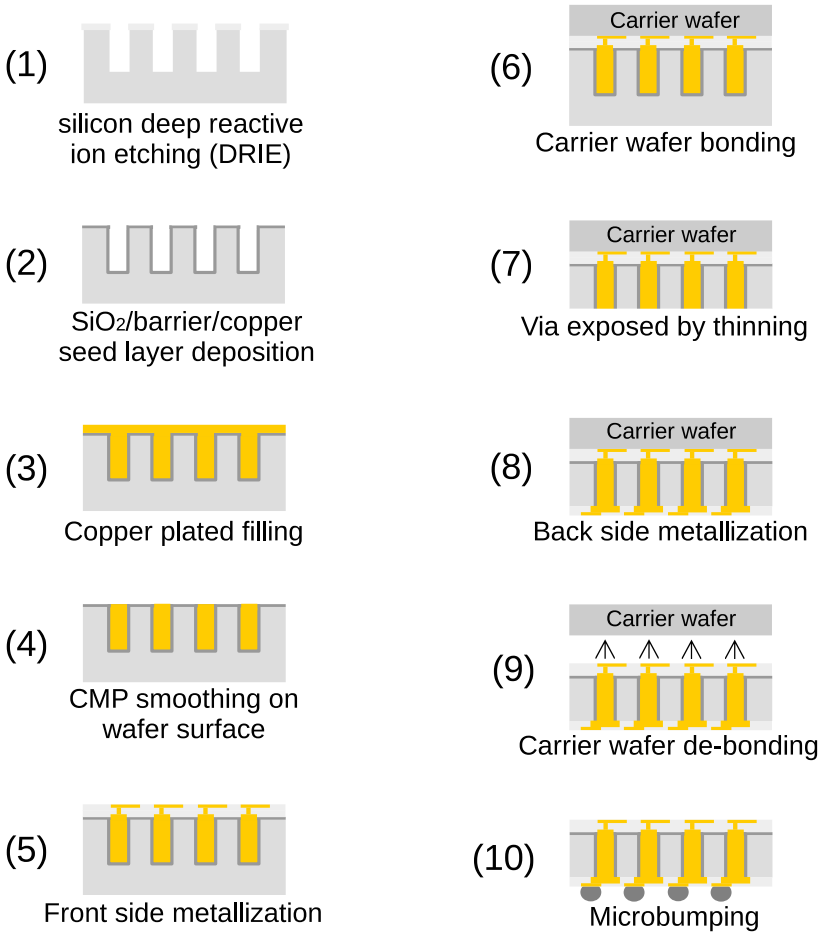


Figure 2.1 Formation of TSVs [22]

After the front-side metallization process, the copper filled vias are thinned at Step (5) to expose the vias at the backside and to bring the interconnects from the front to the back of the silicon substrate. Since the silicon substrate is thin and fragile, a carrier wafer is bonded with either a direct or adhesive bonding technique to ensure mechanical durability during the thinning process at Step (6).

The copper-filled vias are exposed on the back of the wafer with a grinder at Step (7). The back side metallization process is conducted at Step (8), after which the carrier wafer is de-bonded by sliding the wafer off at a high temperature at Step (9). Finally, solder metallization is carried out to form microbumps on the back of the wafer at Step (10).

Because these manufacturing processes occur at an extremely small size, they are quite complicated, particularly the process for creating TSVs. There is the possibility of improper layer deposition during the deposition of the SiO_2 and barrier layers at Step (2), and there is also the risk of improperly filling the vias with copper during electroplating at Step (3). This can lead to defects such as voids and pin holes in the TSVs, which will affect the performance of the 3D stacked ICs [23].

Examples of defective TSVs are shown in Figure 2.2. Pinholes in the SiO_2 layer between the TSV and silicon substrate will cause current leakage, resulting in an undesirable conductive path. Voids occurring inside a TSV increase its resistivity. The dimensions and positions of the voids can also change and affect the electrical parameters of the TSVs [23].

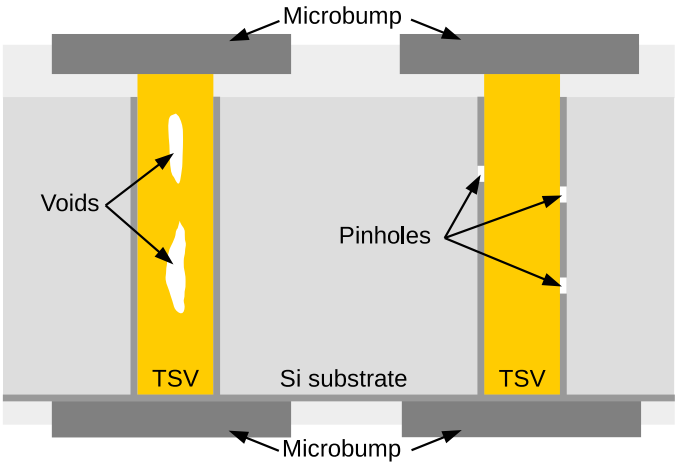


Figure 2.2 TSV defects [23]

2.1.2 Defects in Stacking Processes

In the next stage of the TSV formation process, the wafer is diced and the resulting dies are stacked. The stacking processes can cause additional defects due to high temperature, high pressure, and additional processing steps during stacking [24]. Cracking can also occur due to the forces that occur during loading and back side grinding, as well as in die thinning.

During stacking, open defects can occur at different locations in an interconnect. Examples of such defects are shown in Figure 2.3. An open defect occurs at a TSV in *Die*#1 and *Die*#2 in Figure 2.3, while open defects are also shown in the microbumps between *Die*#1 and *Die*#2, and between *Die*#2 and *Die*#3.

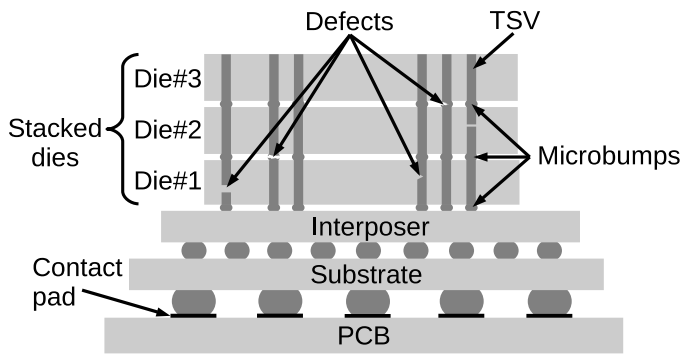


Figure 2.3 Defects occurring during stacking

Non-uniform microbump size, as well as the occurrence of voids or cracks in the microbumps, can affect logic signal transmission capability between the top and bottom dies [25]. The role of microbumps between the stacked dies in a 3D stacked IC is to provide vertical electrical connection. If one or more bumps is significantly smaller than expected, logic signals may not propagate through them.

In addition to size errors, microbump misalignment during the stacking process in any direction (x, y or z) can also affect logic signal propagation through them. Misalignment is due to an offset microbump and results in a smaller contact area for the connection, which can cause higher resistance at the interconnect. TSVs and microbumps between dies must be precisely aligned to maintain good conductivity and minimize their resistance [26]. The bonding quality and yield can also be dramatically reduced by contamination of the bond surface, TSV height variation,

or particles being caught at interconnects between dies. Defects at interconnects should therefore be detected before shipping the ICs to market.

2.2 Defects Caused by Aging

Voids can be formed inside TSVs or microbumps by thermal or mechanical stress during the stacking process and by inexact control during the fabrication of TSVs in 3D stacked ICs. Although the effects of voids on the performance of a system made of the IC are negligible [27], they can create catastrophic defects over the lifetime of the system owing to aging caused by electromigration and stress migration, which reduce the reliability of the IC, especially in the field after shipment to market. An overview of aging is introduced in this section.

2.2.1 Electromigration

In 3D stacked ICs, electromigration can become severe due to dimension mismatches between TSVs, microbumps, and contact pads. Electromigration decreases the reliability of ICs [24] and can cause an open defect. Generally speaking, electromigration is caused by a current flowing through a conductor that produces two forces, to which the individual metal ions in the conductor are exposed, as illustrated in Figure 2.4 [28] - [29].

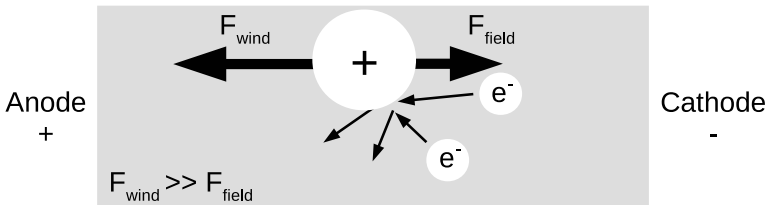


Figure 2.4 The driving forces of electromigration [28]

One is an electrostatic force, F_{field}, that is caused by the electric field strength in the metallic interconnect. Since the positive metal ions are shielded to some extent by the negative electrons in the conductor, this force can be ignored in most cases. The other is an electric wind force, F_{wind}, that is generated by the momentum transfer between conduction electrons and metal ions in the crystal lattice. This force acts in the direction of the current flow and is the main cause of electromigration [28] - [29].

ICs have an intended mean time to failure (MTTF) of at least 10 years [30]. A defect at an interconnect caused by electromigration can result in an IC error. At the end of the 1960s, J. R. Black developed an empirical model to estimate the MTTF of a wire segment. The MTTF can be defined by (2.1) [31],

$$\text{MTTF} = \frac{A}{J^n} \cdot exp(\frac{E_a}{k \cdot T}) \tag{2.1}$$

where A is a constant based on the cross-sectional area of the interconnect, J is a current density, E_a is the activation energy, k is the Boltzmann constant, T is the temperature and n is the scaling factor.

When a current flows through the conductor, electrons release metal atoms from the conductor, and these atoms accumulate at the positive end of the conductor, causing extrusions, while voids are formed at the negative end. The voids increase the resistance of the conductor and can cause an open defect. The extrusions can cause a short defect if they serve as a bridge between adjacent metal lines.

Accumulation of voids is common in electromigration, because small dimensions make it easy for voids to reach a size large enough to cause an open defect. Electromigration induces voids in TSVs and microbumps in 3D stacked ICs. Figure 2.5 shows an example of the defect generation processes in TSVs induced by electromigration. A void in the TSV in Figure 2.5(a) initially grows into a crack on one side of the TSV in Figure 2.5(b). Then, the crack spreads through to the other edge of the TSV in Figure 2.5(c). Ultimately, the crack becomes larger and divides the TSV into two parts in Figure 2.5(d).

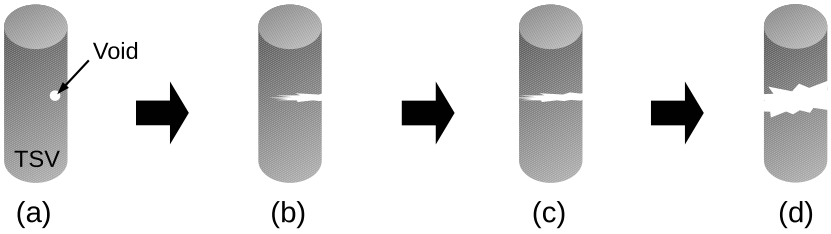


Figure 2.5 Generation of a hard open defect in a TSV by electromigration

2.2.2 Stress migration

In addition to electromigration, discussed in Section 2.2.1, stress migration is a thermal issue affecting the lifetime of 3D stacked ICs that cannot be ignored. Power dissipation in 3D stacked ICs should be well planned because of the existence of thermal hot spots. Power densities in dies and their proximity can cause thermal hot spots in 3D stacked ICs to generate temperatures three times higher than SoCs [32]. The reliability, as well as the electrical characteristics, of 3D stacked ICs is affected by the high temperature.

Stress migration can cause two critical defects. The first is caused by mechanical stresses at the top and bottom edges of the TSV's filling material (copper) and the silicon substrate, respectively. Copper has a coefficient of thermal expansion (CTE) more than five times greater than silicon's. The CTE mismatch between a TSV and the silicon substrate therefore induces mechanical stresses that can lead to higher probabilities of the die cracking and interfacial delamination [33]. The other defect is a crack occurring at the midpoint of a TSV, which can propagate to the other edge of the TSV and affect TSV performance, reducing the reliability of the 3D stacked ICs.

The 3D stacked IC discussed in this paper is fabricated by stacking KGDs connected with TSVs and microbumps. The aging effects of electromigration and the stress migration can occur in both TSVs and microbumps.

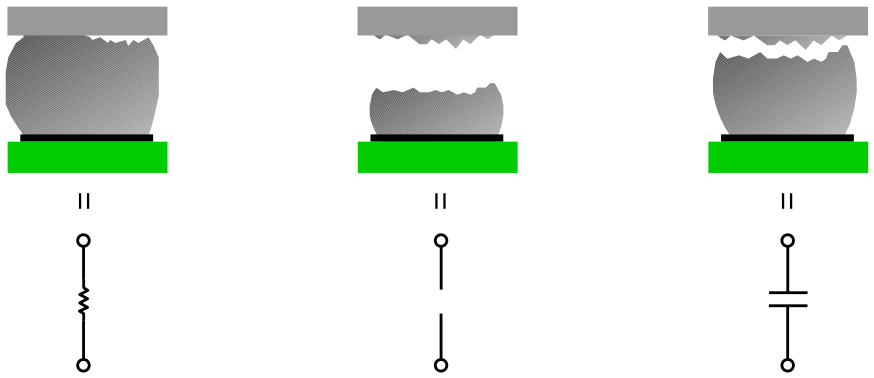
2.3 Models of Selected Open Defects

When KGDs are stacked on top of each die, the open defects shown in Figure 2.3 can occur independently at the interconnects between them. These open defects are classified into *hard* and *soft* open defects. A soft open defect is modeled as a finite resistance path. The interconnect is still partially connected electrically, and logic signals propagate through the defective interconnect with an additional propagation delay time [14]. Soft open defects are caused by a void or a crack in the interconnect, and are also called a weak open defect [14, 16]. In this paper, soft open defects are referred to as resistive open defects.

As the defect grows it can divide the interconnect into two parts. If the gap is sufficiently long, logic signals may not be propagated across the gap; this is modeled as being of infinite resistance and is called a hard open defect in this paper. If the gap is short, the defect is modeled as a capacitance in parallel with a resistance; in such cases, high speed logic signals do propagate through the capacitor [34]. This is called a capacitive open defect in this paper.

Figure 2.6 illustrates the open defects occurring at microbumps between KGDs in a 3D stacked IC. An open defect also occurs in the TSV between KGDs. The resistive open defect is modeled as a resistor, since there is a finite resistance path at the interconnect in Figure 2.6(a). The hard open defect is modeled as an open circuit, since a gap occurs in the microbump as illustrated in Figure 2.6(b). The capacitive open defect is modeled as a capacitor as shown in Figure 2.6(c), since a small gap between the divided parts forms a capacitance.

This paper discusses how to detect the three types of open defects occurring at interconnects between KGDs: (a) resistive open defects, (b) hard open defects, and (c) capacitive open defects.



(a) Resistive open defect (b) Hard open defect (c) Capacitive open defect

Figure 2.6 Models of open defects at a microbumps

2.4 Summary

This chapter discussed the possible causes that can induce open defects at interconnects between KGDs in a 3D stacked IC. An overview of the TSV formation processes and how defects arise in TSVs was presented, along with an overview of the stacking process for KGDs and how defects can arise at interconnects between KGDs.

Defects can also occur in 3D stacked ICs after the ICs are shipped to market. This is due to the aging effects of electromigration and stress migration in ICs. Open defects occurring at interconnects between KGDs in 3D stacked IC during the stacking process are the defects targeted in this paper, and models of such defects have been provided.

Chapter 3 Conventional Interconnect Tests for 3D Stacked ICs

This paper discusses how to detect and locate open defects occurring at interconnects between dies in a 3D stacked IC. The open defects may occur during the stacking processes. Many test methods have been proposed to detect them.

This chapter summarizes test methods to detect open defects after introducing the general 3D stacked IC fabrication processes.

3.1 Test process of 3D stacked ICs

Two kinds of tests are performed before and after the stacking processes of 3D stacked ICs: pre-bond tests and post-bond tests. KGDs are selected using the pre-bond tests before stacking dies. After the KGDs are stacked, they are tested using the post-bond tests.

Generally, a pre-bond test consists of tests of core circuits in dies and tests of TSVs in them. Because defect-free 3D stacked ICs should be made of KGDs, pre-bond tests are indispensable. The tests include die-matching. Dies to be stacked are chosen that satisfy specifications, such as speed or power consumption. Thus, pre-bond tests should be done before stacking because an undetected defective die may harm the entire 3D stacked IC, thus causing a massive loss [40].

After KGDs are stacked, it is imperative to test a partially stacked IC, in which all of the dies have not been stacked yet, and a completely stacked IC. The post-bond tests ensure that the stacked KGDs work as expected and that new defects have not occurred during the stacking processes.

There are many challenges in the post-bond tests of 3D stacked ICs. The newly formed TSVs are tested in the post-bond tests. This paper discusses post-bond tests.

3.2 Post-bond tests for 3D stacked ICs

3.2.1 Boundary scan test method

Interconnects in a 3D stacked IC can be tested by a boundary scan test method as in tests of interconnects between an IC and a printed circuit board (PCB) [5]. Thus, an IEEE 1149.1 test architecture may be implemented within dies inside many kinds of 3D stacked ICs. Because there are many TSVs inside 3D stacked ICs, a long test time is required when the IC is tested by such a test method. Thus, various kinds of design-for-testability (DfT) methods and built-in test circuits have been proposed to shorten the test time [49] - [55].

C. W. Chou *etal.* propose a test integration architecture for 3D stacked ICs [50]. Figure 3.1 shows the test architecture. The test architecture consists of two control interfaces. One is a JTAG/1500 control interface (JTAG/1500 CI), and the other is a 1500 wrapper control interface (1500 WCI), shown in Figure 3.1. They are to control the DFT circuits within dies and handle the test operations of a 3D stacked IC.

C. W. Chou *etal.* denoted that a bottom die in a 3D stacked IC is a master die, and the other dies are slave dies. Each die is provided with the test pads of TCK, TDI, TMS and TDO. Test data are transported from the bottom layer to the upper layer. The following three tests are performed: board-level test when a 3D stacked IC is mounted in the system board, pre-bond test, and post-bond test.

Figure 3.2(a) shows a test operation flow during the board level test. The IEEE 1149.1 test instruction is loaded into an instruction register (IR) of the JTAG/1500 CI. Thus, board-level test patterns are applied. Once it is done, the board-level test is completed.

Figure 3.2(b) shows a test operation flow for the post-bond test. Once the test instruction is loaded into the IR of JTAG/1500 CI, then the test instruction is loaded into an interface instruction register (IIR) for the die testing in Step 2. After that, the test instruction is loaded into the IEEE 1500 test wrapper. Once the test input is provided, the post-bond test is completed.

Figure 3.2(c) shows a test operation flow for a pre-bond test. In the pre-bond

test, two different test operation flows are needed for the slave die and the master die, respectively. For the slave die, a test instruction is loaded into the IIR of the 1500 WCI. Then, the test instruction is loaded into the IEEE test wrappers. Once the test input is provided, the pre-bond test for the slave die is completed. For the master die, the test operation flow is the same as for a post-bond test in Figure 3.2(b). However, Step 2 in Figure 3.2(b) is modified to a "load test instruction into IIR of JTAG/1500 CI" only.

It is examined by simulations using a ITC'99 benchmark circuit by TSMC 0.18μm standard cell library. An area overhead of the proposed JTAG/1500 CI and the 1500 WCI are 0.15% and 0.11%, respectively. The test interfaces are compatible with IEEE 1149.1 standard.

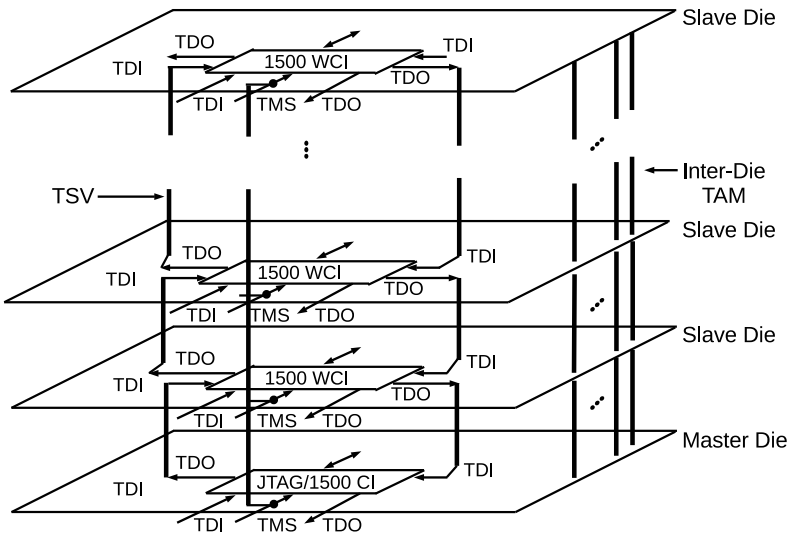


Figure 3.1 Test integration architecture [50]

Y. J. Huang *etal.* propose a built-in self-test (BIST) scheme for the post-bond tests in [53]. The defective interconnects can be detected and diagnosed within a short test time and at a low test cost. Figure 3.3 shows the proposed BIST scheme of 4×4 TSV array for a $Die1$ and a $Die2$. They group them into two logical arrays in which eight TSV signals are from $Die1$ to $Die2$, and the other eight TSV signals are from $Die2$ to $Die1$. The BIST circuit exports the result of pass/fail in a test mode.

Figure 3.4 shows the test operation flow of the BIST, which consists of six

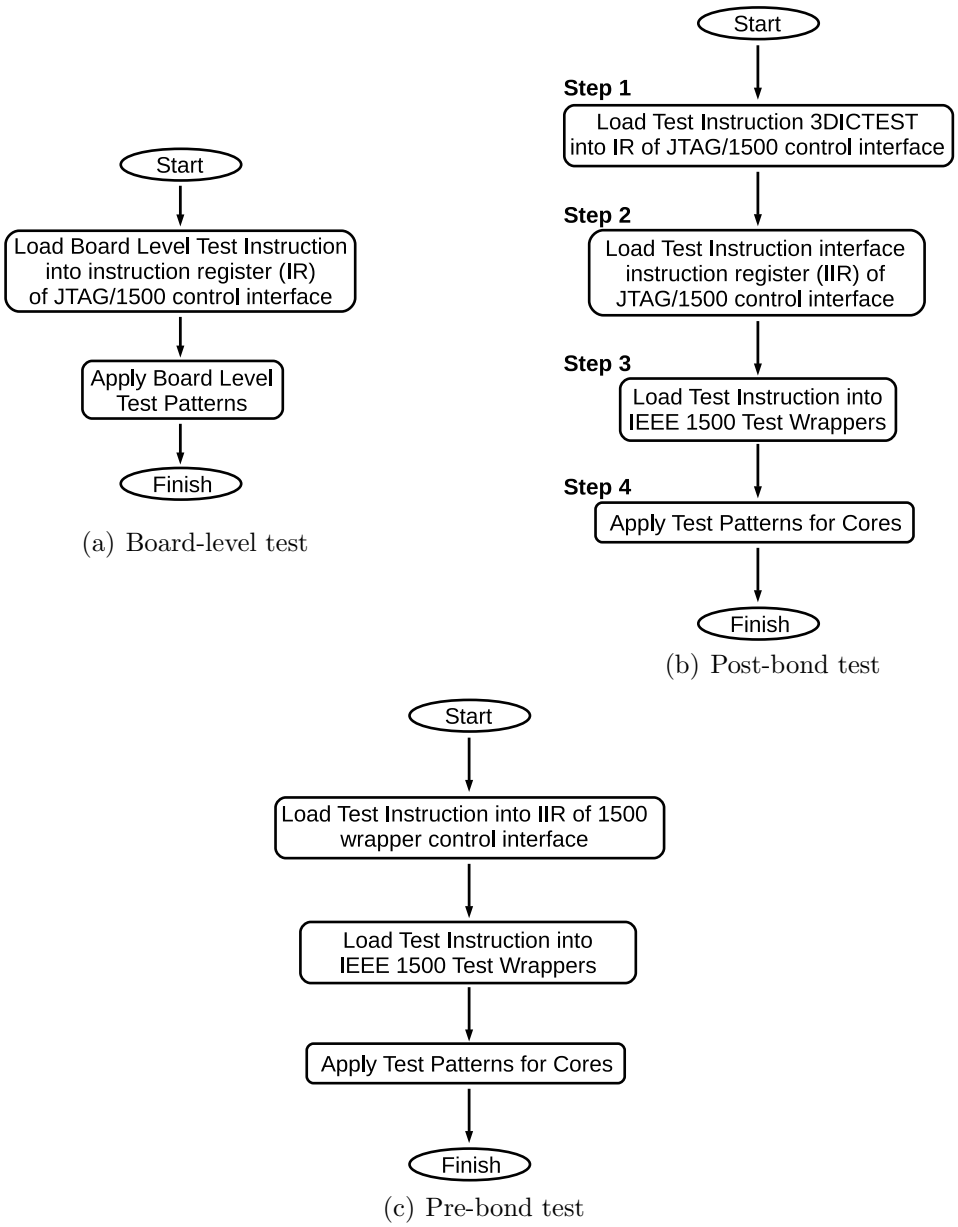


Figure 3.2 Test operation flow [50]

states, namely, MON, GEN_PAT, SHIFT_PAT, CAPTURE_PAT, SHIFT_SIG, and NEXT_ADDR. First, the BIST circuit at a MON waits until a test/diagnosis begins. When the test/diagnosis begins, the BIST circuit moves to a GEN_PAT and generates the test pattern. Once a test pattern is generated, it is shifted to a SHIFT_PAT. In a CAPTURE_PAT, if the BIST circuit is in the test mode, the test pattern is delivered through TSVs. If the TSVs fail, the test procedure stops, or the BIST

circuit is changed to a NEXT_ADDR. The CAPTURE_PAT is repeated and operated until every TSV is tested. If the BIST circuit is in test/diagnosis mode, the test pattern is applied to the other die in the CAPTURE_PAT. In the SHIFT_SIG, the inputs are shifted out to check whether the TSVs are defect-free or not. The SHIFT_SIG is repeated until the test application of the test pattern for TSV under test is completed. If another test pattern is applied, the BIST circuit is returned to a GEN_PAT, and the procedures are repeated. If the test/diagnosis is completed, the BIST circuit is returned to the MON from the NEXT_ADDR.

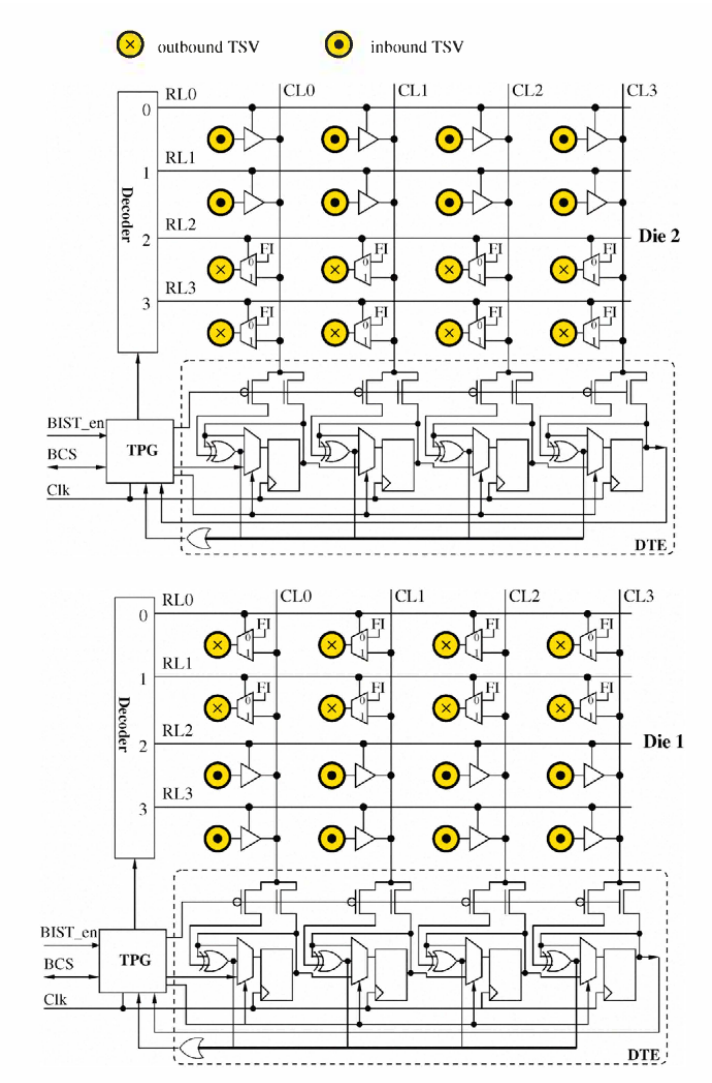


Figure 3.3 BIST scheme [53]

The BIST scheme is examined by simulations using the TSMC 0.18μm standard cell library. The simulation results show that an area overhead decreases as the size of the TSV array increases [53]. However, the area overhead may change for the same TSV array number, but with a different configuration of row *times* column. It is because the shift registers dominate the area of BIST when the number of the column is large. However, the time of the test/diagnosis decreases even as the number of the column increases.

On the other hand, the effectiveness of the proposed BIST scheme is compared with the IEEE 1500 test standard for the area overhead and the test/diagnosis time [53]. The simulation results show that the area overhead of the BIST scheme is smaller than the IEEE 1500 test standard. The time of the test/diagnosis of the BIST scheme is also lower than the IEEE 1500 scheme. The BIST scheme and the IEEE 1500 scheme took 65 test clock cycles and 1024 test clock cycles, respectively.

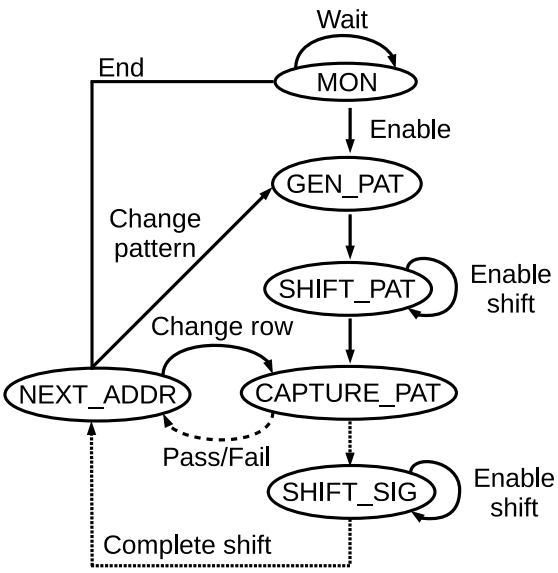


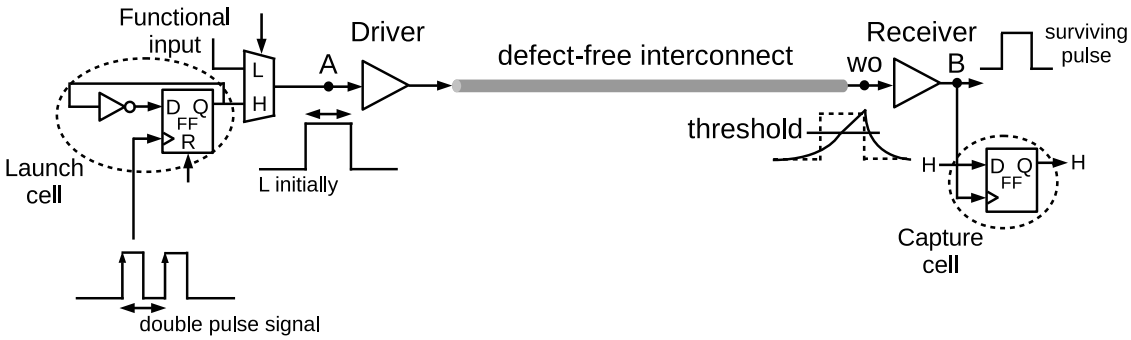
Figure 3.4 Test operation flow [53]

A short defect occurring at the interconnect may be easily detected by the test methods. However, an open defect that generates a timing error may not be detected by the test methods above. The defects that can cause the timing errors may be detected by an electrical test method. Thus, this paper proposes the electrical test method.

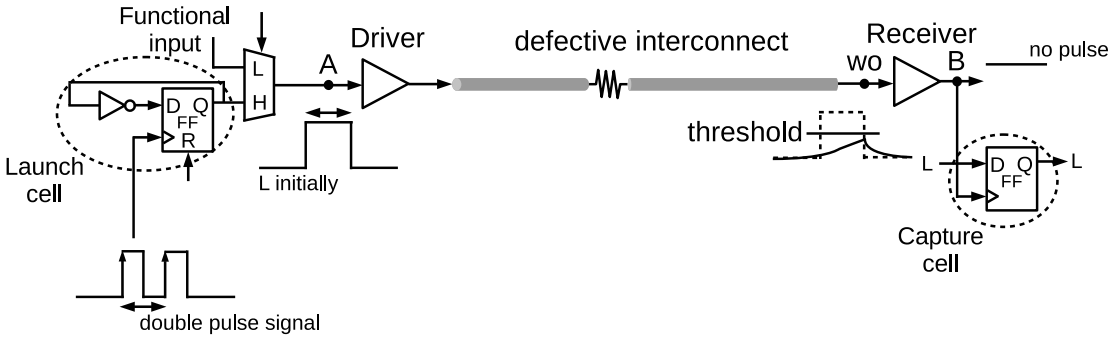
3.2.2 Pulse-Vanishing test

Figure 3.5 shows a test method known as a "Pulse-Vanishing test" [43, 44]. In the tests, a short duration pulse signal is provided to the driving end of an interconnect. The Pulse-Vanishing test can be applied by utilizing the boundary scan cells with the IEEE1149.1 or IEEE 1500 test wrappers.

Figure 3.5 shows a launch cell, which is made to launch the required pulse signal, placed at the driver side. A capture cell that is functioned to detect the arriving pulse signal is placed at the receiver side. Each incorporates a flip-flop.



(a) Defect-free case



(b) Defective case

Figure 3.5 Pulse-Vanishing test method [43]

Both nodes A and B are set at an L level signal before each test cycle by resetting the flip-flop in the launch cell and scan shifting as an L level signal to the capture cell. A double-pulse signal in Figure 3.5 is provided to supply the clock port in the launch cell. Then, the double-pulse signal is converted into the desired single-pulse

signal as a test stimulus by the flip-flop in the launch cell.

The pulsewidth of the test stimulus cannot be controlled accurately when using a single-pulse signal directly, as the pulsewidth may be shrunk or expanded when passing through a routing path from a test controller to a launch cell. However, the time interval between two rising edges in a double-pulse signal is not affected by which when passing through the routing path.

In the capture cell, the clock port of the flip-flop is driven by the output of the receiver. The flip-flop has been initialized to an L level signal before the test cycle, and its input is tied to an H level signal. It will become an H level signal if its clock port is triggered by an arriving pulse signal through the interconnect. Thus, it will indicate a passing condition by an appearance of "surviving pulse" at the receiver in Figure 3.5(a). On the other hand, it will remain as an L level signal if there is no pulse signal through the interconnect. Thus, it will indicate a failing condition by the appearance of "no pulse" at the receiver in Figure 3.5(b).

An open defect occurring at an interconnect is detected by the test method above by examining whether a short pulse signal that applies at the driver side of an interconnect is capable of propagating. A pulsewidth of the short pulse signal is equal to a system clock cycle time, which is typically a high-speed clock cycle. In [43, 44], the clock cycle time is 1GHz. However, by using this test method, it may be difficult to detect an open defect that generates delay time. Also, to pinpoint the open defects with this test method, an accurate time measurement circuit is needed.

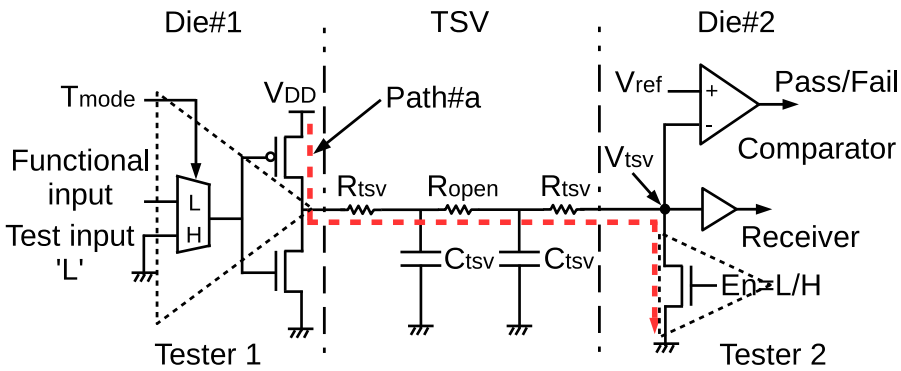
3.2.3 Voltage-divider-based test

A built-in test circuit and a test method based on a voltage divider test is proposed in [42] to test if a die-to-die interconnect has a resistive open defect. The test method is used for a post-bond test. The test circuits generate the voltage of a TSV, V_{tsv}, to detect a resistive open defect occurring in a TSV.

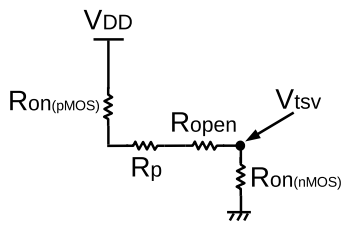
Figure 3.6(a) shows the test circuit. It is consists of $Tester1$ and $Tester2$. A test circuit of $Tester1$ is made of a multiplexer to select a test mode. A test circuit of $Tester2$ is made of a comparator and an nMOS transistor. The nMOS transistor is added between the input of receiver and the ground.

The test circuits work in two modes. The one is a normal mode, and the other is a test mode. In the normal mode, the multiplexer in the $Tester1$ selects a functional input, and the enable signal in the $Tester2$ is an L level signal. During this mode, the TSV drives the receiver in $Die\#2$. In the test mode, the multiplexer in the $Tester1$ selects a test input, which is tied to an L level signal. The enable signal in the $Tester2$ is an H level signal. Thus, current flows from the supply voltage terminal, V_{DD}, along the current path, $Path\#a$, in Figure 3.6(a).

When the current flows as shown in Figure 3.6(a), a voltage divider circuit is obtained, which is shown in an equivalent circuit in Figure 3.6(b). Thus, the V_{tsv} is fed to a negative input of the comparator as shown in Figure 3.6(a). A positive input of the comparator is driven by a constant reference voltage signal, V_{ref}, as shown in Figure 3.6(a). When a resistive open defect occurs in a TSV, it is judged by comparing the V_{tsv} with the V_{ref}.



(a) Test circuit



(b) Equivalent circuit

Figure 3.6 Voltage-divider-based test method [42]

The V_{tsv} depends on a parasitic resistor, R_p, a resistive open defect, R_{open}, on-resistance of pMOS in $Tester1$, $R_{on_{pMOS}}$, and on-resistance of nMOS in $Tester2$,

$R_{on_{nMOS}}$. Thus, the following two outcomes will be produced to judge if a resistive open defect occurs at a TSV under test:

(1) V_{tsv} is higher than V_{ref} if the TSV is defect-free

(2) V_{tsv} is lower than V_{ref} if the TSV is defective

It is reported in [42] that the V_{tsv} should be designed to drop below $0.8V_{DD}$ in case of a defect-free TSV, so that the comparator can indicate the resistive open defect. The nMOS transistor in the $Tester2$ is designed based on the smallest defect resistance being targeted. In [42], it is stated that the smallest R_{open} being targeted is 1 kΩ. Thus, a ratio of W/L = 3/1 is selected and sufficient in order to detect R_{open} of 1 kΩ. The maximum R_{open} that can be detected by the test method is 10 kΩ [42].

In this test method, because V_{tsv} depends mainly on the magnitude of R_{open}, the size of nMOS for each interconnect and V_{ref} may need to be selected carefully to set up a proper threshold value. This may present a challenge, because it must be determined for each interconnect. Also, a circuit made of a comparator and an nMOS transistor is added to each interconnect causing a large area overhead.

3.2.4 X-ray computed tomography

Open defects at interconnects in a 3D stacked IC may be caused by a void or a crack in a TSV or in a micro bump. Test methods based on a non-destructive imaging technique of an X-ray with computed tomography (CT) scan have been proposed in order to detect such defects [45] - [48].

Figure 3.7 shows a basic setup of a 3D X-ray CT scan. A 3D X-ray system consists of an X-ray source, a rotating stage and an X-ray detector, shown in Figure 3.7. The test method is implemented at different fabrication process steps of TSVs to inspect a TSV structure. X-ray CT is able to construct a 3D view of a TSV by capturing series of 2D X-ray images at different and regular angles. The captured images are processed mathematically and superimposed to construct a 3D view of the TSV. By capturing X-ray images at different angles, defect shapes, sizes, and distributions can be observed, because they are displayed as a virtual cross-section or a slice view of the TSV.

There were studies that implemented the X-ray CT scan as a test method to detect a defect at an interconnect in 3D stacked ICs. V. N. Sekhar *etal*. employed 3D X-ray CT scan analysis to inspect high density TSV structures fabricated with different diameters and depths [45]. They indicate that it is possible to observe the defect shapes, the sizes, and the distributions through detailed 3D X-ray CT scan analysis by the virtual cross-section at the desired location.

S. H. Lau *etal*. revealed that an X-ray nanotomography provided a new way in non-destructive characterization of defects in a defect analysis [46]. They have demonstrated sub-50 nm resolution tomographic 3D imaging for defect localization in multi-level interconnect structures with a hard X-ray nanotomography system.

L. W. Kong *etal*. reported that visualization of voids and copper extrusion in TSVs under different annealing conditions was greatly enhanced using the X-ray microscopy [48]. They have investigated the changes in copper extrusion and induced voiding in TSVs of 25 μm depth and 4-5 μm diameter that result from annealed dies at 225 ° and 300 °.

Despite the capability to detect defects at interconnect in 3D stacked ICs, one disadvantage of the test method is that such detection may be time consuming and prone to false alarms resulting in a significant yield loss.

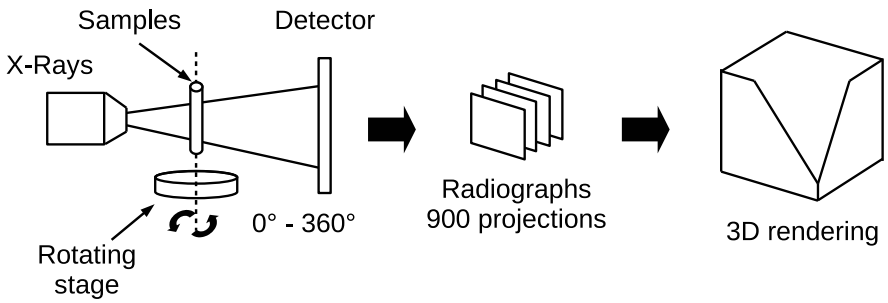


Figure 3.7 3D X-ray CT scan setup [45]

3.3 Summary

This chapter provides an overview of conventional interconnect tests for 3D stacked ICs. They can be classified in the following two types: pre-bond tests and post-bond tests.

Generally, pre-bond tests are performed to a die before being stacked in order to examine if it is a KGD. Thus, a defective die that may harm the entire stacked IC may be detected. During the stacking process, an open defect may occur at an interconnect among KGDs. It is also indispensable to perform testing after the stacking processes to detect such defects. Thus, the post-bond tests are performed. Only the post-bond tests are discussed in this paper.

Chapter 4 Built-in Electrical Interconnect Test Circuit Using Boundary Scan Flip Flops

An IEEE 1149.1 test circuit is included in dies inside many 3D stacked ICs so that interconnects between KGDs can be tested easily, and 3D stacked ICs made of dies containing a test circuit are the devices under test (DUTs) in this chapter. A built-in supply current test circuit is proposed in this chapter to detect open defects at interconnects in 3D stacked ICs using a quiescent supply current that flows during the tests. Boundary scan flip flops in the dies are used to provide test signals to the interconnect to be tested.

Until now, built-in supply current test circuits have been proposed together with electrical test methods using test circuits. After summarizing the current test circuits and test methods in Section 4.1, a revised test circuit and method are proposed in Section 4.2. The circuit and method are evaluated experimentally and by SPICE simulation. The evaluation results are discussed in Section 4.3.

4.1 Built-in quiescent supply current test circuits

Electrical interconnect test methods have been proposed by T. Konishi *etal.* to detect open defects at interconnects between dies in 3D stacked ICs [35] - [37]. These test methods are based on a quiescent supply current that is made to flow only through the interconnect under test with boundary scan flip flops embedded in the dies. Open defects can occur at interconnects made of TSVs or at microbumps between the dies, and these are the defects to be detected in this paper.

A setup for testing a 3D stacked IC made of three KGDs is shown in Figure 4.1. The control signals for the test method, TDI, TCK, TMS and $TRST$, are provided to the DUT from an external tester as shown in Figure 4.1. Two kinds of source voltage, V_{DDC} and V_{DDIO}, are supplied to the IC and are provided to core circuits in the dies and the input/output interface circuits in them, respectively.

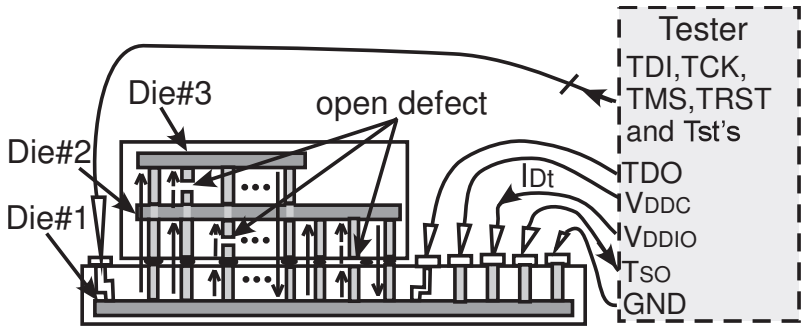


Figure 4.1 Test setup for a 3D stacked IC

Typically, no quiescent supply current flows through interconnects between dies in 3D stacked ICs, so dies testable by these methods are designed by a DfT method such that a quiescent current can flow during the interconnect tests using the boundary scan flip flops embedded in the dies. Since each of the interconnects is scanned and electrically tested with boundary scan flip flops, the test is called an ET-Scan test [37].

The test principle for an electrical interconnect test method proposed in [35] is shown in Figure 4.2. This test is based on a quiescent supply current, I_{Dt}, that is made to flow through the interconnect under test as shown in Figure 4.2. The dies are designed such that a quiescent supply current can flow through an interconnect during the tests. As shown in Figure 4.2, the anodes of the diodes in the electrostatic discharge (ESD) input protection circuits are connected to the test terminal, Tst, of a 3D stacked IC. This means that the test method proposed in [35] does not add any circuits to the 3D stacked IC, althrough because input protection capability may be reduced by the modification of the ESD input protection circuits, IC designers may not wish to modify them. Another test method has therefore been proposed that does not modify the input protection circuits [36].

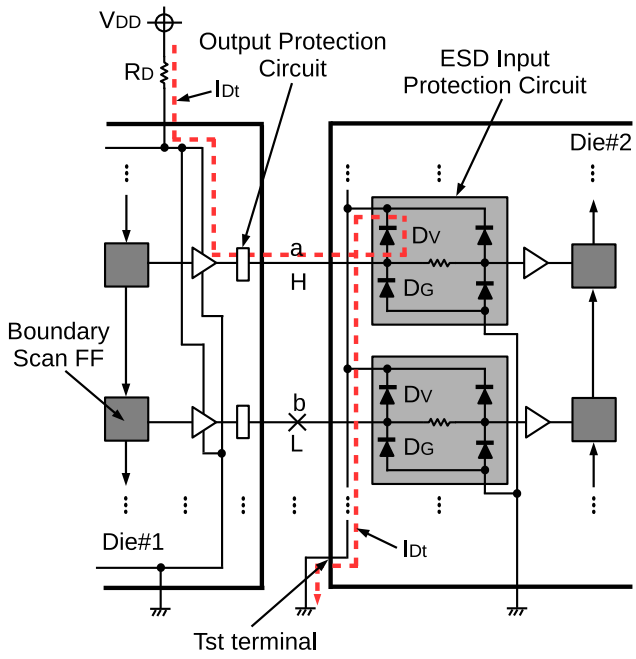


Figure 4.2 Test principle for electrical test method [35]

The test principle for the electrical interconnect test method proposed in [36] is shown in Figure 4.3. To make a quiescent supply current, I_{Dt}, flow through the interconnect under test, a built-in test circuit made of nMOS switches is added to each of the input interconnects to be tested; this is shown as the Added Circuit Block in Figure 4.3.

Generally speaking, current measurements result in higher test cost than voltage measurements, since relatively expensive equipment is needed to measure currents. An electrical test method that measures voltages during the tests has been proposed [37].

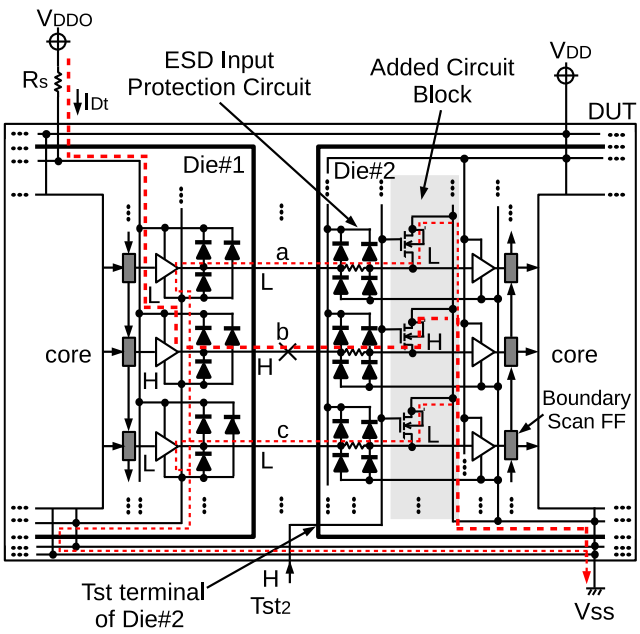


Figure 4.3 Test principle for electrical test method [36]

The test principle for the test method proposed in [37] is shown in Figure 4.4. The interconnects between $Die\#1$ and $Die\#2$ are tested in Figure 4.4. An nMOS switch is added to the output terminal of any protection circuit for each input interconnect in the dies so these interconnects can be tested by the proposed test method. The MOSs are depicted in circuit block CBa in Figure 4.4. The source terminals for all of the nMOS switches are connected to the T_{SOP} terminal of the IC. The Tst terminal of each die in the DUT is connected to the gate terminals of the added nMOS switches.

Whenever the IC is tested, a test circuit made of a switch, Swt, that toggles between a resistor, R_c, at side sb and an high (H) level signal at side sa, is connected to the T_{SOP} terminal. The expensive measurement equipment necessary to measure I_{Dt} can be replaced by a voltage measurement device because the quiescent voltage across R_c, V_{Rc}, is measured instead of I_{Dt}.

An H level signal is provided by the IEEE 1149.1 test circuit only to the interconnect under test-the targeted interconnect (e.g., interconnect b in Figure 4.4)-whereas low (L) level signals are provided to interconnects other than the targeted one. The

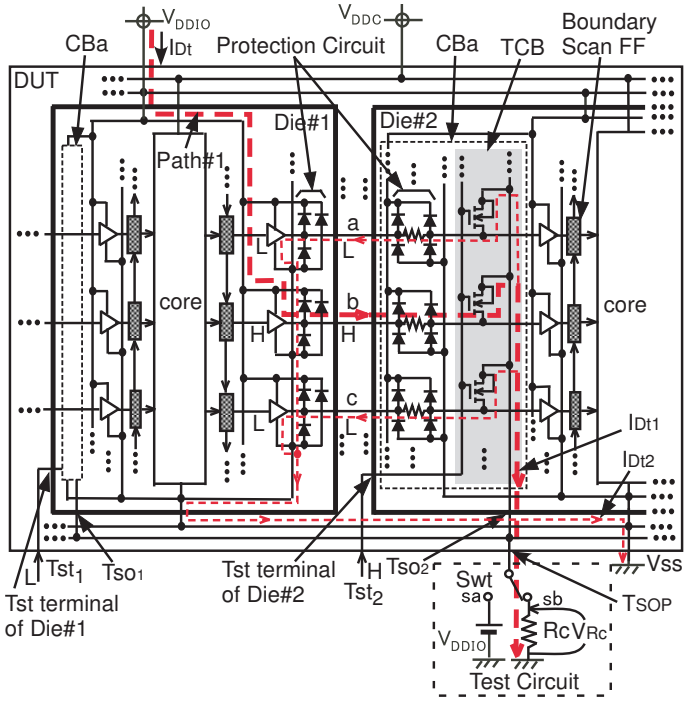


Figure 4.4 Test principle for electrical test method [37]

test input signal application creates a quiescent supply current path, $Path\#1$, of I_{Dt} from V_{DDIO} to GND, when an H level signal is provided to the Tst terminal of $Die\#2$, Tst_2.

If either a hard or capacitive open defect occurs at the targeted interconnect, I_{Dt} will not flow. If a resistive open defect occurs at the interconnect, a smaller quiescent I_{Dt} than the defect-free ICs will flow. Thus, if (4.1) is satisfied, there is an open defect at the targeted interconnect:

$$\mathrm{I_{Dt}} \leq \mathrm{I_{th}} \tag{4.1}$$

where I_{th} is the threshold value specified from the variation of I_{Dt} from the defect-free ICs.

The quiescent voltage across R_c, V_{Rc}, is defined by (4.2).

$$\mathrm{V_{Rc}} = \mathrm{R_c} \cdot \mathrm{I_{Dt}} \tag{4.2}$$

If (4.3) is satisfied, there is an open defect at the targeted interconnect:

$$\mathrm{V_{Rc}} \leq \mathrm{V_{th}} \tag{4.3}$$

where V_{th} is the threshold value specified from the variation of V_{Rc} of the defect-free ICs.

However, some part of I_{Dt} may flow into interconnects other than the targeted one as shown in Figure 4.4. Some part of I_{Dt} in the figure flows as I_{Dt2}, since an L level signal is provided to interconnects other than the targeted one. Thus, I_{Dt} is expressed by (4.4).

$$\mathrm{I_{Dt}} = \mathrm{I_{Dt1}} + \mathrm{I_{Dt2}} \tag{4.4}$$

I_{Dt2} depends on the number of interconnects between dies connected to the targeted interconnect. As it increases, a large reverse current I_{Dt2} may flow, and the changes in I_{Dt} caused by an open defect may decrease. As a result, a resistive open defect of small resistance may not detected by the test method. Many threshold values for the tests should also be prepared before the tests, since the thresholds depend on the number of the interconnects through which I_{Dt2} flows. The test circuit and the test method should be therefore revised.

4.2 A revised built-in quiescent supply current test circuit

In this paper, a new built-in test circuit has been developed that prevents I_{Dt2} in Figure 4.4 from flowing in tests [56]. The circuit is shown as circuit block CBb in Figure 4.5. A diode is added to the source terminals of the nMOS switches to prevent I_{Dt2} in Figure 4.4 from flowing in the tests, as shown in Figure 4.5. The cathode terminals of all of the diodes are connected to the Tso terminal of the IC and a Tst terminal is added to the die connected to the gate terminals of the nMOS switches.

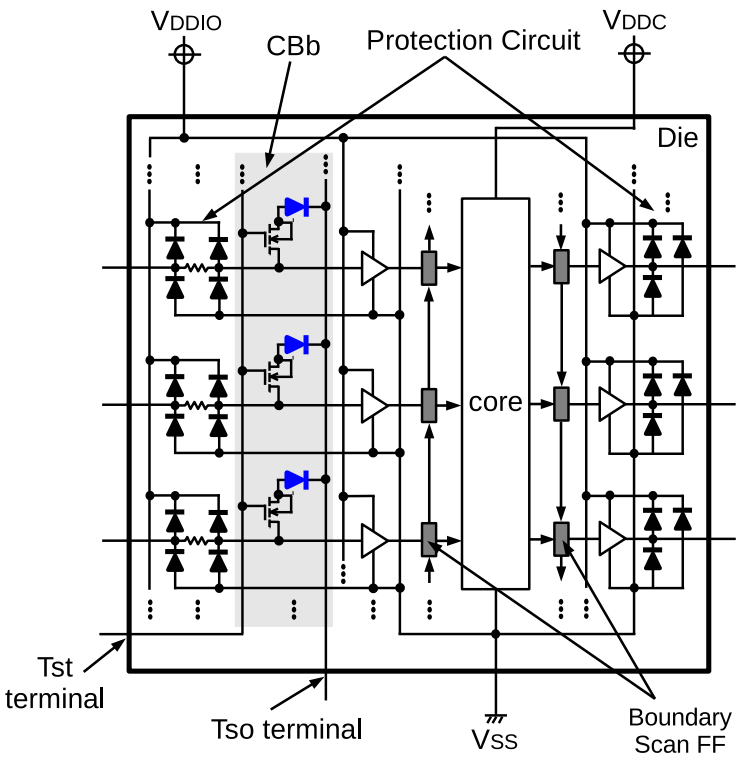
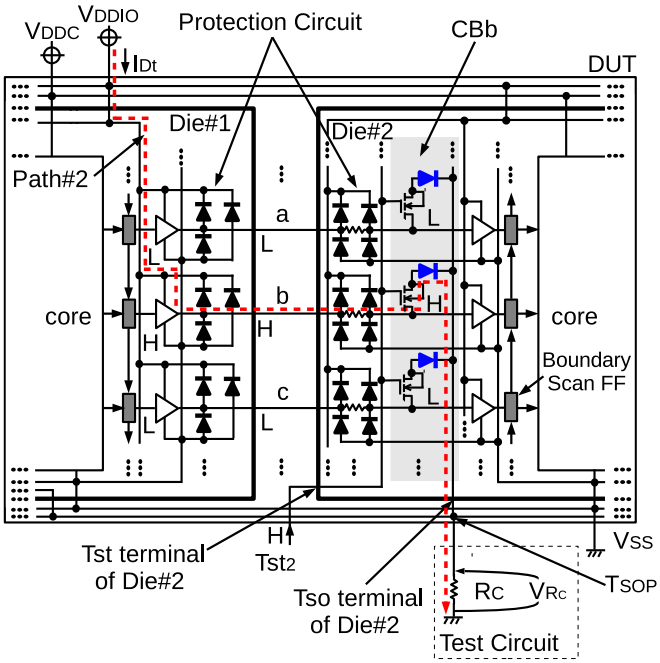


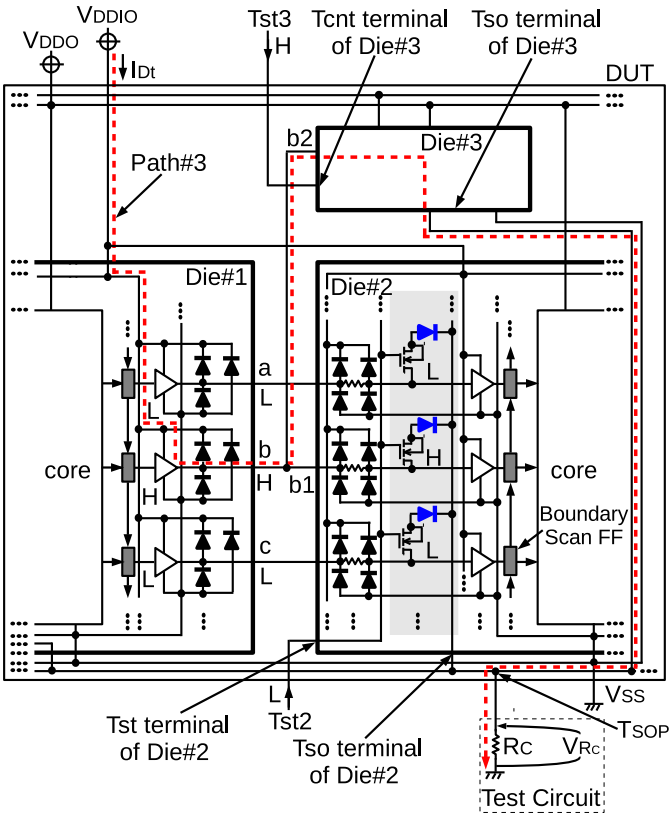
Figure 4.5 New built-in test circuit

When a 3D stacked IC is made of two dies, the interconnects between them are modeled as the circuit shown in Figure 4.6(a). The principle for an electrical interconnect test method is shown in Figure 4.6(a) with the revised built-in test circuit for interconnects between $Die\#1$ and $Die\#2$.

Whenever a defect-free IC is tested, I_{Dt} will flow only along the current path, $Path\#2$, shown in Figure 4.6(a), since only the diode that is on $Path\#2$ is turned on. Whenever either a hard open defect or a capacitive open defect occurs at the targeted interconnect b in Figure 4.6(a), no current will flow. When a resistive open defect occurs at the interconnect, a smaller I_{Dt} will flow than in the defect-free ICs. Since the current flows through only one interconnect at a time, a defective interconnect can be located by examining when (4.3) is satisfied.



(a) Test principle for an interconnect without fan-out branch



(b) Test principle for an interconnect connecting to more than two dies

Figure 4.6 Test principle of new test method

Interconnect b in Figure 4.6(a) is tested by the following procedures:

(1) Provide L and H level signals to the test terminal of $Die\#1$, Tst_1, and the test terminal of $Die\#2$, Tst_2, respectively.

(2) Provide an H level signal and L level signals to b and to interconnects other than b, respectively, from the boundary scan cell in $Die\#1$ so that I_{Dt} can flow along the current path, $Path\#2$, from V_{DDIO}.

(3) Measure V_{Rc} in the test circuit connecting to the T_{SOP} terminal of the 3D stacked IC.

(4) Compare the measured V_{Rc} to V_{th}. If (4.3) is satisfied, there is an open defect at b.

More than two dies may be connected with only one interconnect in 3D stacked ICs, as shown in Figure 4.1. In this case, the interconnect among them is modeled as an interconnect with a fan-out branch as shown in Figure 4.6(b).

Whenever interconnects connecting more than two dies are tested, an H level signal is provided to the Tst terminal of only one of the dies to which the fan-out branches of the targeted interconnect are connected. For example, an input interconnect of $Die\#3$, $b2$, in Figure 4.6(b) is tested by the following procedures:

(1) Provide L level signals to the test terminal of $Die\#1$ and $Die\#2$, Tst_1 and Tst_2, and an H level signal to the test terminal of $Die\#3$, Tst_3, respectively.

(2) Provide an H level signal and L level signals to b and to interconnects other than b, respectively, from the boundary scan cell in $Die\#1$ to make I_{Dt} flow along the current path, $Path\#3$, from V_{DDIO}.

(3) Measure V_{Rc} in the test circuit connecting to the T_{SOP} terminal of the 3D stacked IC.

(4) Examine whether the measured V_{Rc} satisfies (4.3), and if (4.3) is satisfied, there is an open defect at $b2$.

A defective interconnect can be located by the electrical interconnect test, since an H level signal is outputted to only one interconnect and is provided to the Tst terminal of only one die. For example, if (4.3) is satisfied only in the cases of

$Tst_2 = H$ and $Tst_3 = L$ in Figure 4.6(b), there is an open defect at the input interconnect of $Die\#2$, $b1$. If the condition is satisfied only in the cases of $Tst_2 = L$ and $Tst_3 = H$, then the defect occurs at $b2$. If (4.3) is satisfied in both of the cases, then the defect occurs at b.

Interconnects between dies inside a DUT and the primary output pins of the IC are tested by measuring V_{Rc}, as shown in Figure 4.6. Such interconnects are tested by connecting to ICs containing a circuit block CBb, depicted in Figure 4.5, and providing test input signals for this test method from boundary scan flip flops in the dies.

Open defects can occur at interconnects between dies simultaneously. In this test method, only one interconnect is tested at a time, so even if an open defect occurs at more than one interconnect, the defective interconnects are both detected and located by this test method.

Only dies that have been judged as KGDs in pre-bond tests are stacked. The testable designed circuit block CBb in a die is easily tested during the pre-bond test by providing V_{DDIO} to only one of the input interconnects and providing no signal to the others. During the test, V_{Rc} is measured after connecting the test circuit to the Tso terminal of the die with test probes attached to it, so CBb in the die can be tested from the measured V_{Rc}.

4.3 Evaluation of the revised built-in test circuit

4.3.1 Testability examination by simulation

The layout of a die containing CBb was designed using 0.18μm CMOS technology from Rohm Co., Ltd., to examine the feasibility of tests based on this test method. An inverter chain circuit of 16 stages is the core circuit in the die.

Input and output protection circuits used in the die design were initially adopted from the CMOS cell library distributed by VDEC in the University of Tokyo, Japan. Prior to the IC prototyping by Rohm Co., Ltd., however, both of the protection circuits in the designed die were replaced by protection circuits from the IC foundry. The specifications for the protection circuits are not available to the public.

The test circuit was examined by SPICE simulations to determine whether an open defect occurring at interconnects between two dies as shown in Figure 4.6(a) was detected by the test method described in Section 4.2. The following two voltage sources were supplied to the dies whose voltages were specified by the CMOS process: $V_{DDIO} = 3.3$ V, $V_{DDC} = 1.8$ V.

A SPICE netlist was extracted from the layout of the designed die depicted in Figure 4.7 with the extraction tool $Virtuoso$ produced by Cadence. A SPICE netlist of the simulation circuit shown in Figure 4.8 was coded by merging the extracted netlist and adding a parasitic resistor R_p of 2 mΩ and a parasitic capacitor C_p of 242 fF [38] to each of the interconnects, as shown in Figure 4.8. A resistor R_c of 300 Ω was used in the test circuit. The selection of R_c is discussed in Section 4.3.3. The sizes of the nMOS switch and the diode in the designed CBb were: $l = 360$ nm and $w = 28$ μm.

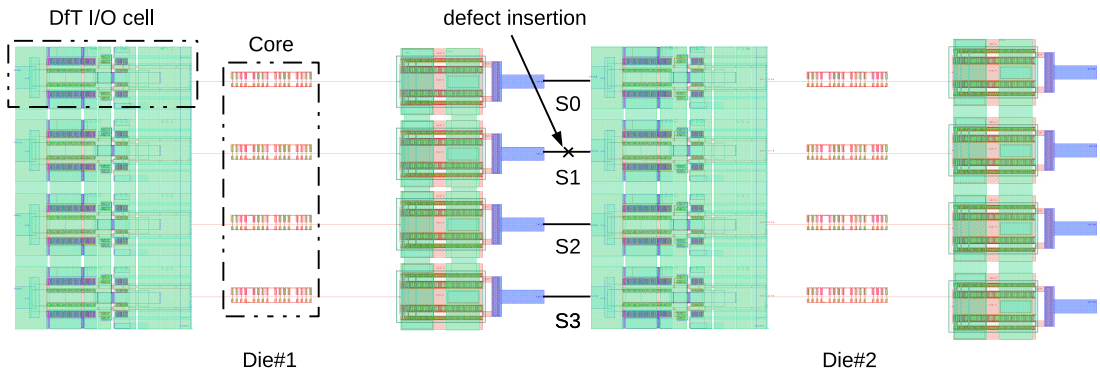


Figure 4.7 Layout extracted from the designed die

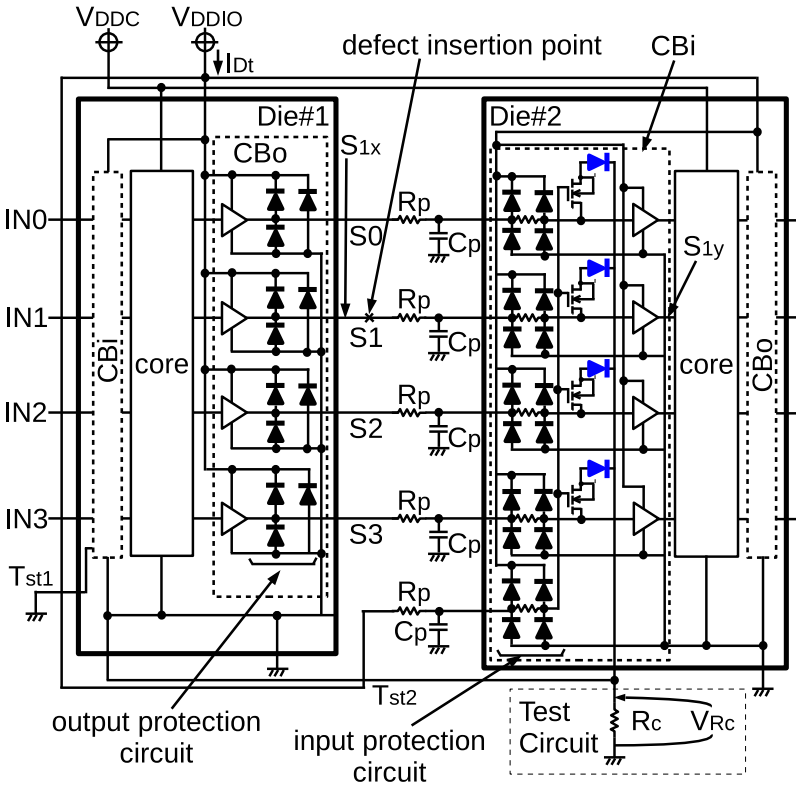


Figure 4.8 Simulation circuit

A hard open defect was inserted at interconnect $S1$ by adding a resistor R_f of 1 TΩ to the coded netlist to determine whether a hard open defect was detectable. A resistive open defect and a capacitive open defect were inserted to $S1$ by adding a resistor R_f and a capacitor C_f to the netlist, respectively.

Input signals to $IN0$, $IN1$, $IN2$, and $IN3$ in the evaluations are shown in Figure 4.9. The test vectors were provided to the circuit per Ts. An IEEE 1149.1 test circuit is not included in the designed dies. However, by providing the test vectors to $IN0$, $IN1$, $IN2$, and $IN3$, the same operation can be achieved as for a circuit made of dies in containing IEEE 1149.1 test circuits.

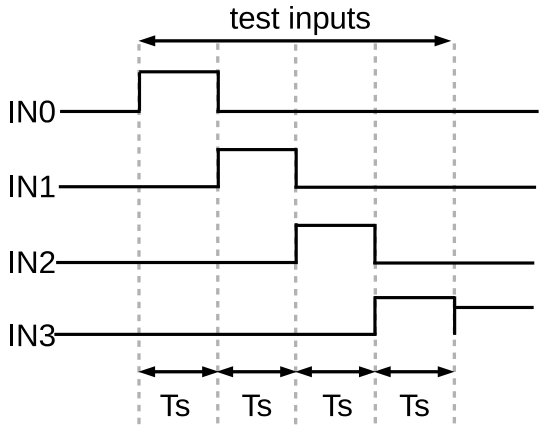
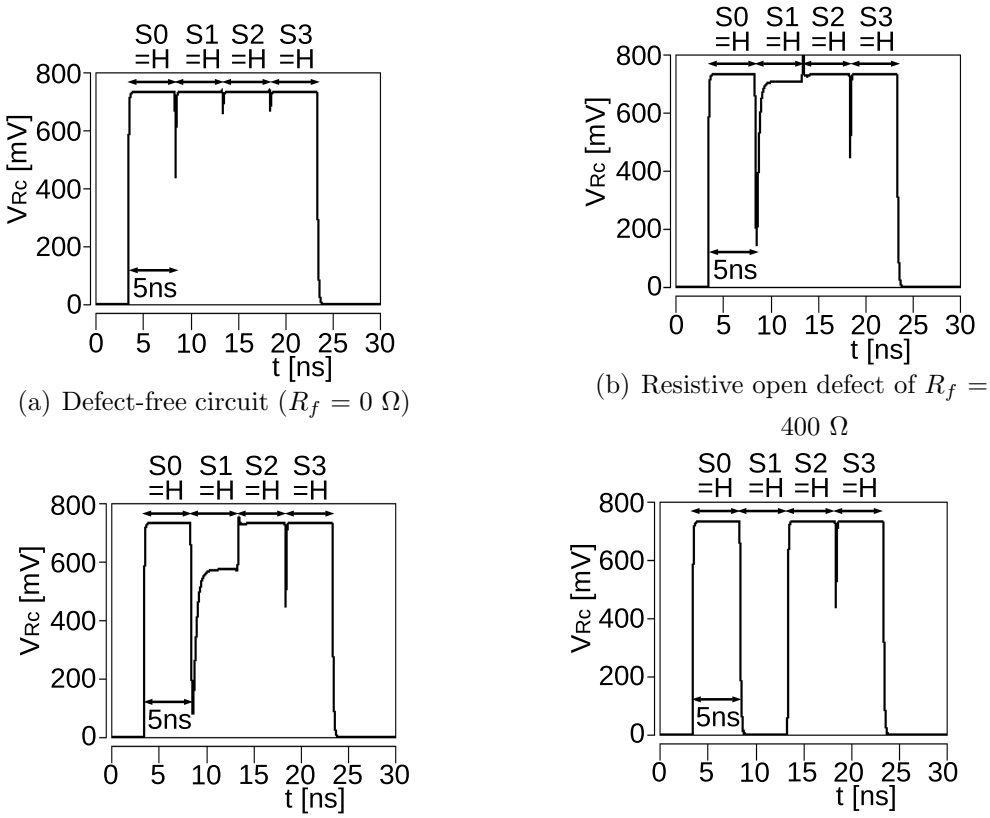


Figure 4.9 Test input signals

The V_{Rc} waveforms of the defect-free circuit and three defective circuits are shown in Figure 4.10. I_{Dt} stops flowing whenever an L level signal is provided to the targeted interconnect following an H level signal that has been provided to it. An H level signal is then provided to another interconnect and I_{Dt} resumes flowing. After V_{Rc} decreases at the beginning of each test input application, large V_{Rc} appears, as shown in Figure 4.10.

When a resistive open defect of $R_f = 400\ \Omega$ occurs at $S1$, almost the same V_{Rc} appears as in Figure 4.10(a) before providing a test input signal to the next interconnect, as shown in Figure 4.10(b). The open defect may thus not be detected by the test method. On the other hand, the hard open defect and the resistive open defect of $R_f = 750\ \Omega$ at $S1$ are detected by the test method, since a smaller V_{Rc} appears than for the defect-free circuit before providing a test input signal to the next interconnect. Defects can be detected at a test speed of 200 MHz, since $Ts =$ 5 nsec.



(a) Defect-free circuit ($R_f = 0\ \Omega$)

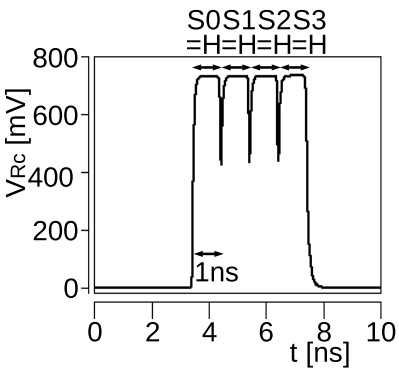
(b) Resistive open defect of $R_f = 400\ \Omega$

(c) Resistive open defect of $R_f = 750\ \Omega$

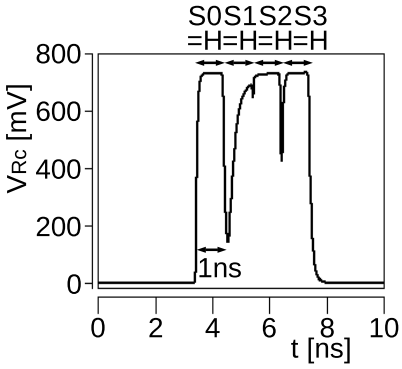
(d) Hard open defect ($R_f = 1$ TΩ)

Figure 4.10 Tests for resistive open defects at $Ts = 5$ nsec

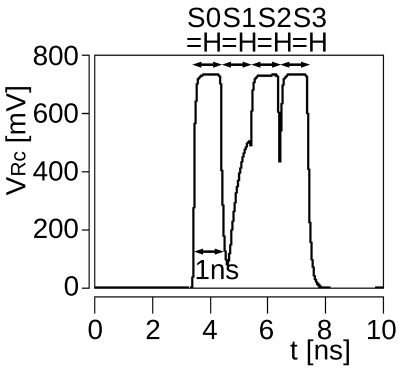
Simulation results for $Ts = 1$ nsec are shown in Figure 4.11. An H level signal is provided to $S2$ before quiescent V_{Rc} appears when $S1 = H$ as shown in Figure 4.11(b) and Figure 4.11(c). It is therefore impossible to detect open defects by means of quiescent V_{Rc}s at test speeds higher than 1 GHz.



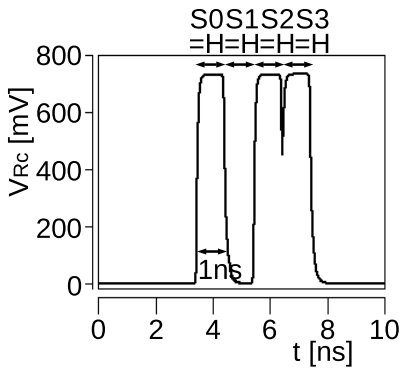
(a) Defect-free circuit ($R_f = 0\ \Omega$)



(b) Resistive open defect of $R_f = 400\ \Omega$



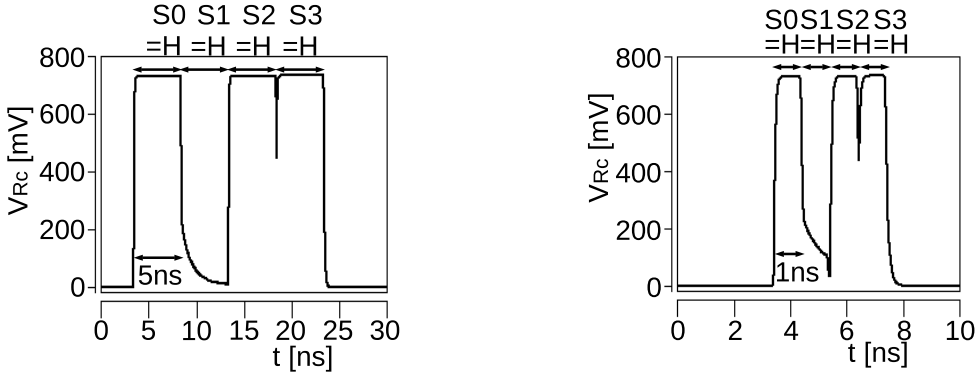
(c) Resistive open defect of $R_f = 750\ \Omega$



(d) Hard open defect ($R_f = 1$ TΩ)

Figure 4.11 Tests for resistive open defects at $Ts = 1$ nsec

When a capacitive open defect of $C_f = 0.47$ pF occurs at $S1$, V_{Rc} appears as in Figure 4.12. A supply current from V_{DDIO} begins to flow through $S1$ to charge C_f when an H level signal is outputted to $S1$ after providing an L level signal to $S0$. As C_f is charged, I_{Dt} shrinks and V_{Rc} decreases as shown in Figure 4.12(a). When C_f is fully charged, I_{Dt} stops flowing and V_{Rc} becomes zero. However, at a higher test speed, an H level signal is provided to $S2$ before a quiescent V_{Rc} appears when $S1 = H$ as shown in Figure 4.12(b), since C_f cannot be charged quickly.



(a) Test speed of 200 MHz (b) Test speed of 1 GHz

Figure 4.12 Tests for capacitive open defects of $C_f = 0.47$ pF

The V_{Rc} waveform of a defective circuit, in which a capacitive open defect of $C_f = 2$ pF occurs at b, is shown in Figure 4.13. As shown in Figure 4.13, the capacitive open defect cannot be detected by measuring quiescent V_{Rc} at a test speed of 1 GHz.

As the capacitance increases, it takes a longer time to charge C_f fully. When C_f is fully charged, V_{Rc} becomes zero. Since V_{Rc} of zero satisfies (4.3), the defect is detected by the test method, which means that open defects of large capacitance will be detected by reducing the test speed. As shown in Figure 4.12, a capacitive open defect of $C_f \leq 0.47$ pF will be detected at a test speed of 200 MHz.

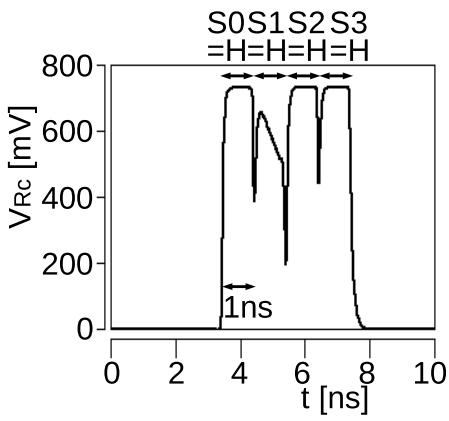
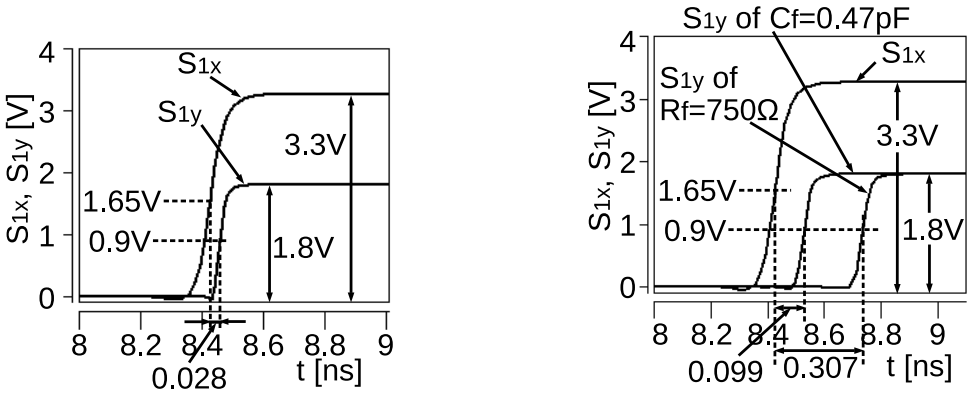


Figure 4.13 Test for capacitive open defect of $C_f = 2$ pF at a test speed of 1 GHz

Voltage waveforms at $S1_x$ and $S1_y$ in the simulation circuit with $Tst_2 = L$ are shown in Figures 4.14 and 4.15. It is observed from Figure 4.14 that the resistive open defect of $R_f = 750\ \Omega$ and the capacitive open defect of $C_f = 0.47$ pF at $S1$ generate additional propagation delay times of 279 psec and 71 psec, respectively. These defects are detected by the test method at the test speed of 200 MHz, as shown in Figure 4.10(c) and Figure 4.12(a).



(a) Defect-free circuit (b) Defective circuit

Figure 4.14 Propagation delay times

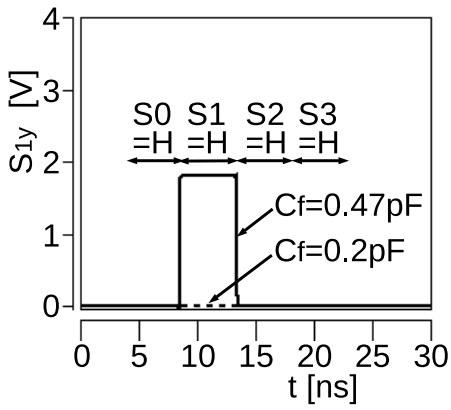


Figure 4.15 Faulty effects of a capacitive open defect

An H level signal does not propagate to $S1_y$ in the case of a capacitive open defect of $C_f = 0.2$ pF, as shown in Figure 4.15, and will thus be detected by measuring the logical error. However, an H level signal propagates to $S1_y$ in case of a capacitive open defect of $C_f \geq 0.47$ pF, which means that a capacitive open defect of $C_f \geq 0.47$ pF cannot be detected by measuring the logic values, since no logical errors

appear. The defect of $C_f = 0.47$ pF is detected by the test method at a test speed of 200 MHz, as shown in Figure 4.12(a). It thus appears that capacitive open defects undetectable by measuring logic values are detected by this test method.

4.3.2 Testability examinations by experiments

A layout of an IC was designed for this study and prototyped. Figure 4.16 shows the layout of the prototype IC. A PCB circuit made of the IC was built to examine experimentally the method's testability with the built-in test circuit. The PCB circuit is shown in Figure 4.17.

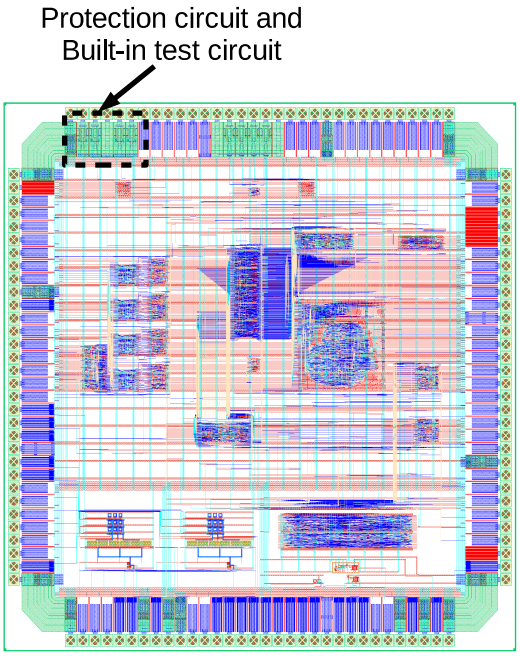


Figure 4.16 Layout of prototyped IC

The experimental circuit is not identical to the simulation circuit shown in Figure 4.8, because the IC foundry has not released the specifications for CBi and CBo in Figure 4.17 to the public. The I_{Dt} that flows in tests mainly depends on CBo. CBo of SSIs are opened to the market, so the circuit shown in Figure 4.17 was made of SSIs to determine testability.

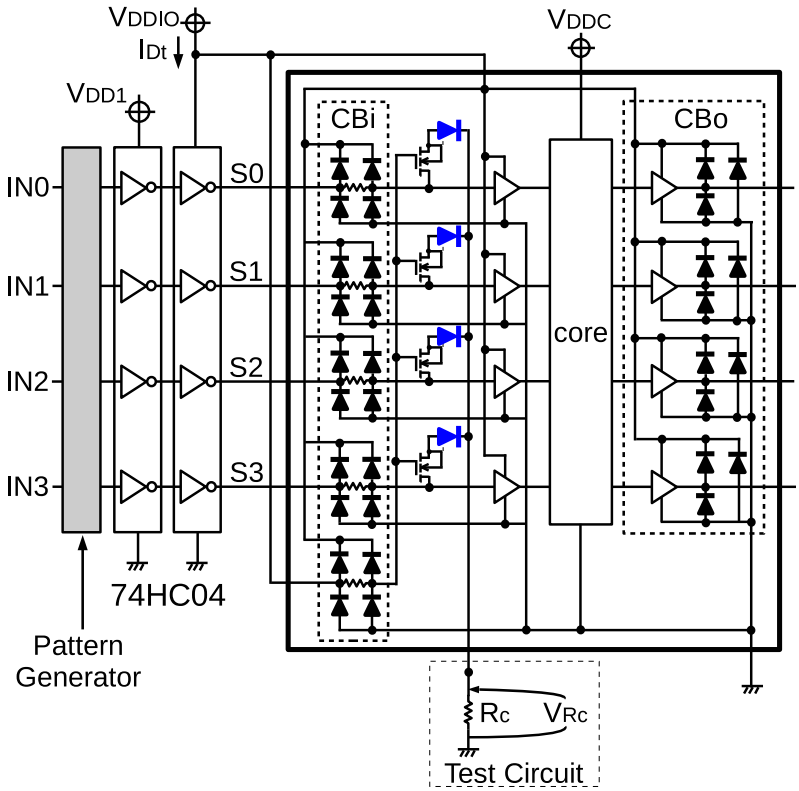


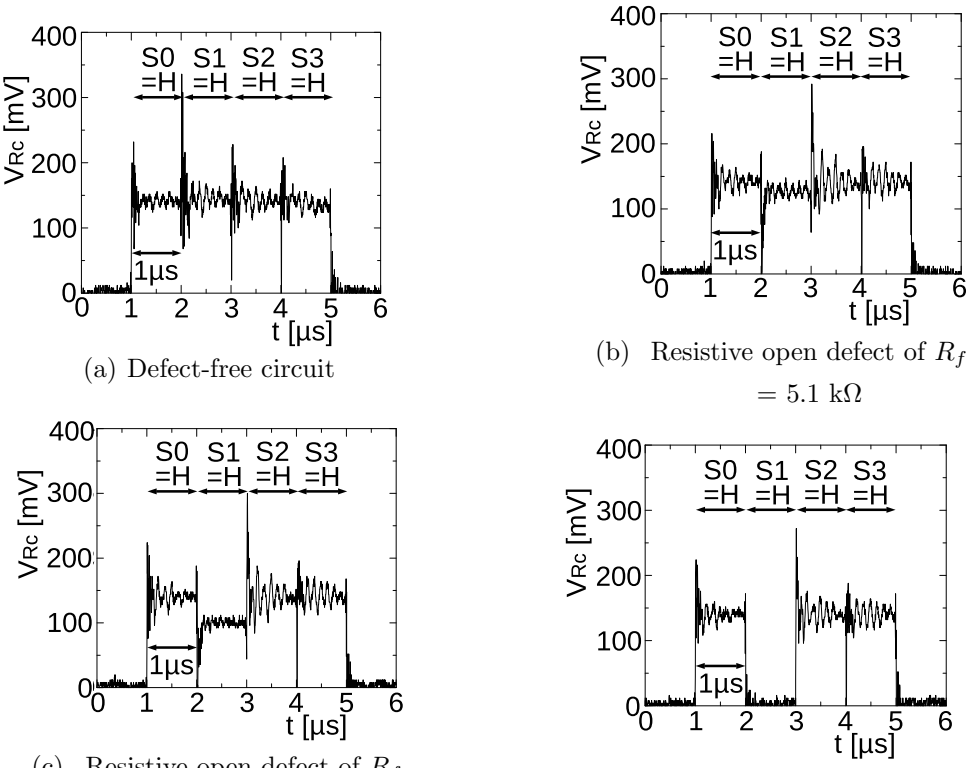
Figure 4.17 Experimental circuit

V_{DDIO}, V_{DDC}, and R_c in the experiments are 3.3 V, 1.8 V and 300 Ω, respectively, which are the same as those used in the simulations described in Section 4.3.1. The input signals of $IN0$, $IN1$, $IN2$, and $IN3$ were provided from a pattern generator. TTL compatible signals were generated with the generator, so a logic level shifter made of inverter gates was inserted into the experimental circuit with $V_{DD1} = 5$ V supplied.

A hard open defect was inserted at $S1$ by eliminating the interconnect from the defect-free circuit. A resistive open defect and a capacitive open defect were inserted at $S1$ by adding a resistor R_f and a capacitor C_f to the interconnect in defect-free circuit, respectively.

Input vectors shown in Figure 4.9 were provided to $IN0$, $IN1$, $IN2$, and $IN3$ per Ts of 1 μsec. V_{Rc} was measured with a Tektronix, DPO3014 digital oscilloscope. The experimental results of the defect-free and defective circuits are shown in Figure 4.18. A resistive open defect of $R_f = 7.5$ kΩ and a hard open defect occur at $S1$. They can be detected by the test method, since a smaller V_{Rc} appears, as shown

in Figures 4.18(c) and 4.18(d). A V_{Rc} that is almost the same as the one in the defect-free circuit appears at $S1 = H$ as shown in Figure 4.18(b), so a resistive open defect of $R_f = 5.1$ kΩ may not be detected by this test method.



(a) Defect-free circuit

(b) Resistive open defect of $R_f = 5.1$ kΩ

(c) Resistive open defect of $R_f = 7.5$ kΩ

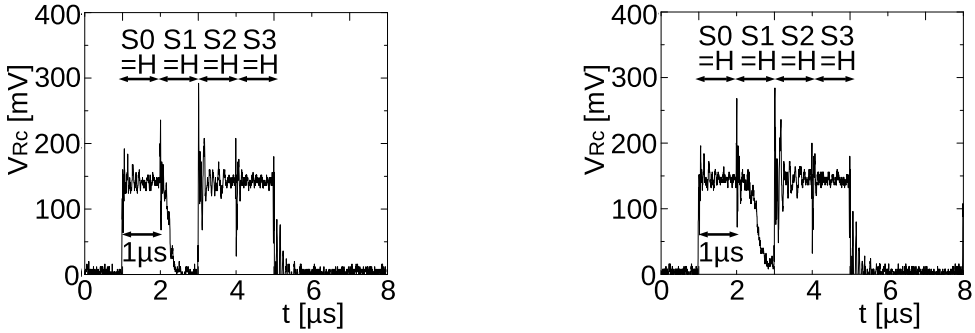
(d) Hard open defect

Figure 4.18 Tests for resistive open defects at $Ts = 1$ μsec

Capacitive open defects of $C_f = 47$ pF and $C_f = 100$ pF were both detected by the test method, as shown in Figure 4.19. As the capacitance increases, it takes a longer time for C_f and C_p to be charged fully. Such larger capacitance defects can be detected by a large Ts.

V_{Rc}s in the experimental results were smaller than the corresponding ones obtained in the simulation results because the actual models of circuit blocks CBi and CBo in the prototype IC differ from the ones in the simulation circuits. The reason for the discrepancy is the inability of user to access the explicit model blocks of the prototype IC provided by the IC foundry.

To validate the experimental results denoted above, SPICE netlists of the circuit



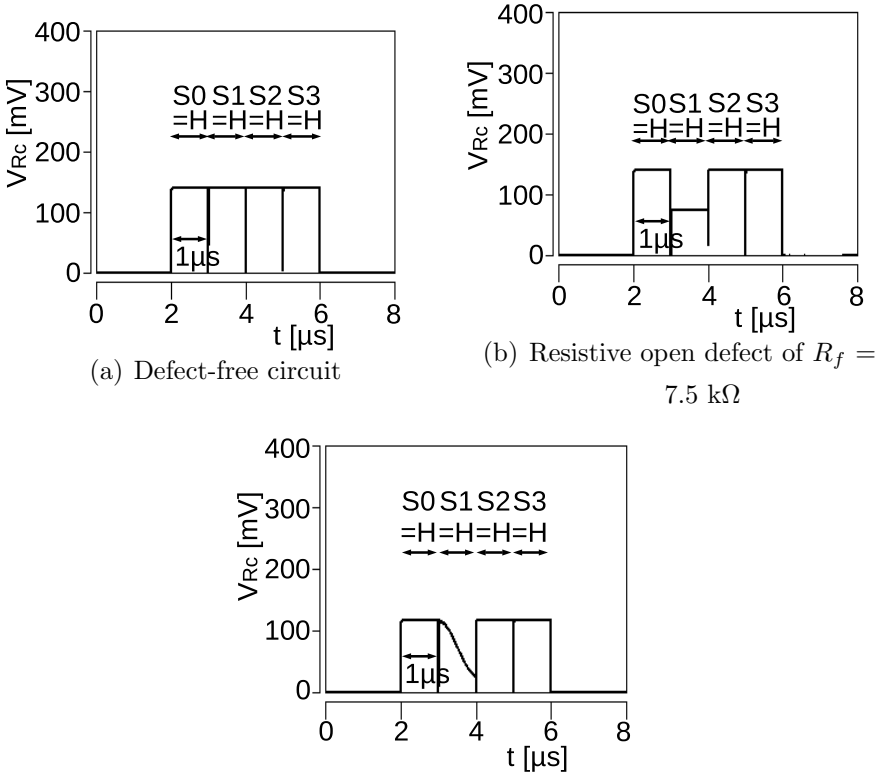
(a) Capacitive open defect of C_f = 47 pF

(b) Capacitive open defect of C_f = 100 pF

Figure 4.19 Tests for capacitive open defect at $Ts = 1$ μsec

in Figure 4.17 were coded along with a netlist of 74HC04 distributed by NXP Co., Ltd., and the netlist of the designed die. The sizes of the MOSs in the output buffer gates inside 74HC04 were adjusted so that almost the same V_{Rc} could appear as in Figure 4.18(a). A resistive open defect of $R_f = 7.5$ kΩ and a capacitive open defect of $C_f = 100$ pF were added to the netlist. The simulation results are shown in Figure 4.20.

As shown in Figure 4.20, almost the same results were obtained from the simulation as from the experimental results of Figures 4.18(c) and 4.19(b). The small difference is caused by the difference in CBi between the designed IC and the prototype IC. This validates by SPICE simulation that the test method detects defects inserted into the experimental circuit.



(a) Defect-free circuit

(b) Resistive open defect of R_f = 7.5 kΩ

(c) Capacitive open defect of C_f = 100 pF

Figure 4.20 SPICE simulation of circuit made of resized CBo at $Ts = 1$ μsec

4.4 Considerations

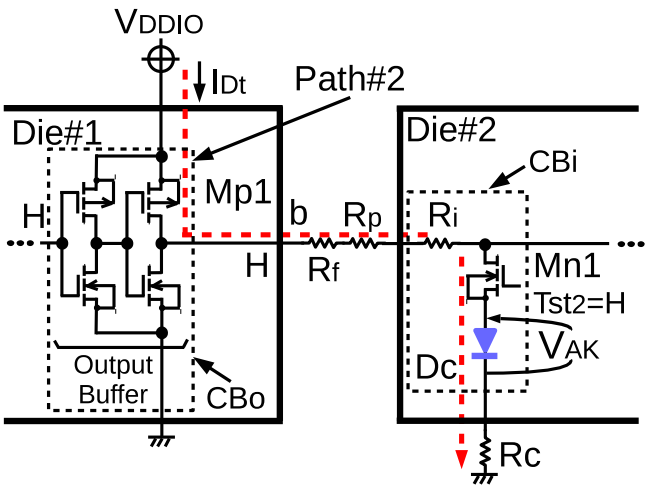
4.4.1 Resistance selection for current measurement

The testability of a resistive open defect depends on process variation and R_c. This section further examines the testability of resistive open defects using the test method.

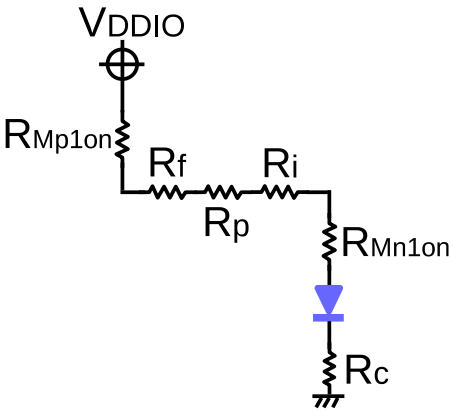
An equivalent circuit of the current path of $Path\#2$ in Figure 4.6(a) is shown in Figure 4.21(a). In the figure, Ri is a resistor in the input protection circuit depicted in Figure 4.8. An output buffer in CBo consists of six stages of inverter chain. When an H level signal is provided, an L level signal is an input signal of the final stage of the inverter chain. Thus, an H level signal is outputted from the output buffer gate in CBo to b.

An L level signal and an H level signal are provided to the gate terminals of $Mp1$

and $Mn1$ in the test of b, respectively. When the circuit is defect-free and $R_c = 0\Omega$, drain currents of less than 115 mA and 6.8 mA flow when both $Mp1$ and $Mn1$ operate in the triode mode. It can be found from the $I_{Dt} - V_{DS}$ characteristics curve of the $Mp1$ and $Mn1$, shown in Figures 4.22(a) and (b), respectively. In Figures 4.10 and 4.12, I_{Dt} of 2.5 mA flows when a defect-free circuit is tested, because V_{Rc} becomes approximately 750 mV across R_c of 300 Ω by (4.2). It means that $Mp1$ and $Mn1$ indeed operate in the triode mode. Thus, $Mp1$ and $Mn1$ are modeled as a resistor, and the equivalent circuit is simplified to a circuit made of resistors and a diode, shown in Figure 4.21(b).

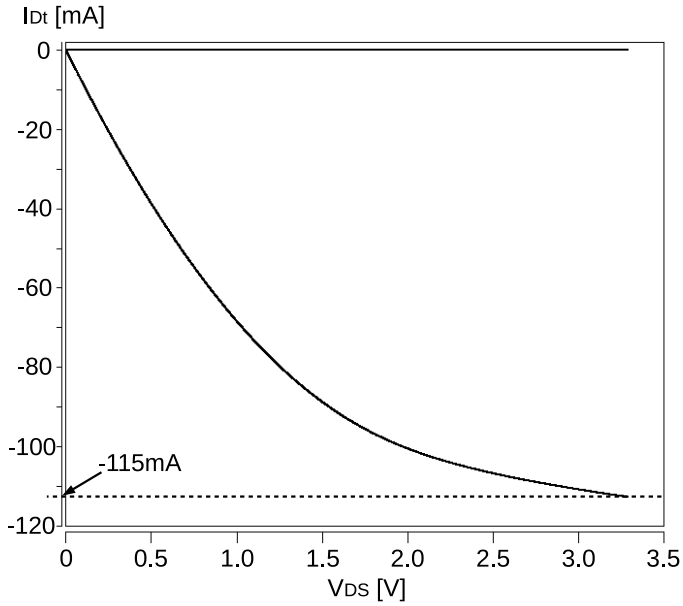


(a) Equivalent circuit

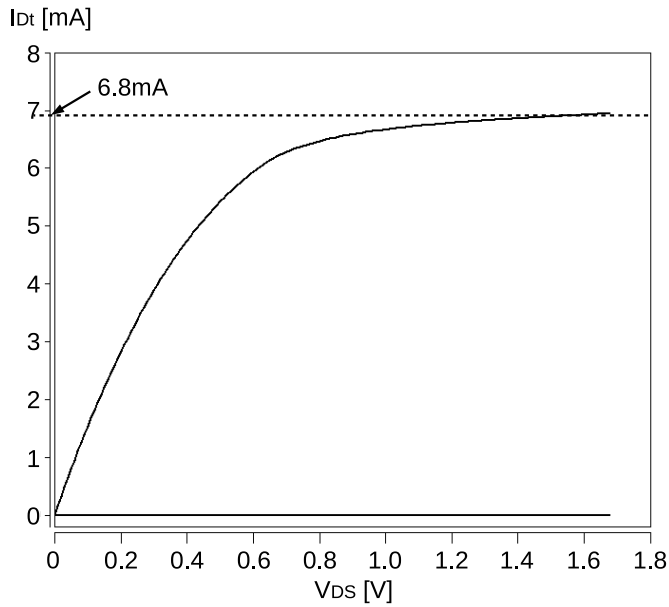


(b) Simplified circuit

Figure 4.21 Circuit model



(a) $I_{Dt} - V_{DS}$ characteristics curve of $Mp1$



(b) $I_{Dt} - V_{DS}$ characteristics curve of $Mn1$

Figure 4.22 $I_{Dt} - V_{DS}$ characteristics curve

I_{Dt} is found from the intersection of the Ohm's law characteristics and an $I_{Dt} - V_{AK}$ characteristic curve of the diode, shown in Figure 4.23. The characteristics of Ohm's Law are defined by (4.5), and the $I_{Dt} - V_{AK}$ characteristic curve of the diode is defined by (4.6).

$$\mathrm{I_{Dt}} = \frac{V_{DDIO} - V_{AK}}{R_c + R_p + R_i + R_{Mp1on} + R_{Mn1on}} \tag{4.5}$$

$$\mathrm{I_{Dt}} = \mathrm{I_S} \cdot (e^{\frac{V_{AK}}{V_T} - 1}) \tag{4.6}$$

where I_S is the saturation current of a diode. R_{Mp1on} and R_{Mn1on} are the on-resistances of $Mp1$ and $Mn1$. V_T is the thermal voltage, which is defined by (4.7).

$$\mathrm{V_T} = \frac{kT}{q} \tag{4.7}$$

where k, T and q are the Boltzmann's constant, an absolute temperature in operation and the charge of an electron, respectively.

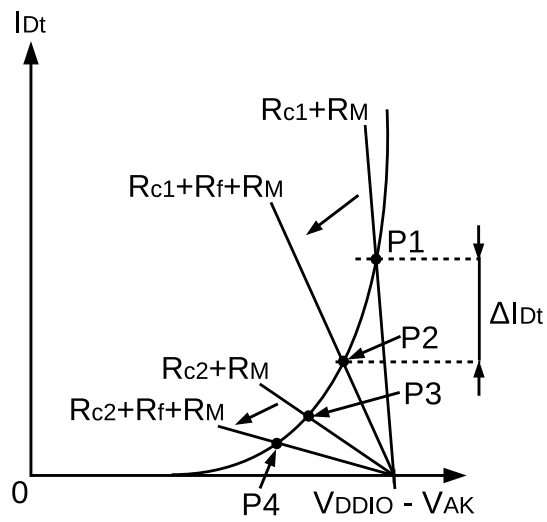


Figure 4.23 Dependability of I_{Dt} from R_c

Whenever a hard open defect or a capacitive open defect occurs, I_{Dt} does not flow, and V_{Rc} becomes zero independently of R_c. However, V_{Rc} depends on R_c for resistive open defects. In the case of R_c, whose resistance is R_{c1}, I_{Dt} specified by $P1$ in Figure 4.23 flows. R_M in the figure is the sum of R_p, R_i, R_{Mp1on} and R_{Mn1on}. If a resistive open defect whose resistance is R_f occurs at b, I_{Dt} flows, whose value is defined as an intersection $P2$ of the $I_{Dt} - V_{AK}$ characteristic curve and the line defined by (4.8).

$$\mathrm{I_{Dt}} = \frac{V_{DDIO} - V_{AK}}{R_c + R_p + R_i + R_{Mp1on} + R_{Mn1on} + R_f} \tag{4.8}$$

The smaller the total resistance, the steeper the line and vice versa.

The difference of I_{Dt} between the defect-free IC and the defective one, ΔI_{Dt}, depends on R_c. When a resistor of R_{c2} larger than R_{c1} is used, I_{Dt} specified by $P3$ flows in the defect-free IC. If a resistive open defect of R_f occurs at b, I_{Dt} specified by $P4$ in Figure 4.23 flows. As shown in Figure 4.23, ΔI_{Dt} to R_{c2} is smaller than R_{c1}.

Resistive open defects are detected by means of V_{Rc}. Because V_{Rc} is defined by (4.2), it is found from Figure 4.23 that, as R_c become smaller, ΔV_{Rc}, which is defined as the difference from V_{Rc} in the defect-free ICs, becomes larger. Thus, R_c should be as small as possible in order to detect resistive open defects of small resistance. However, as R_c becomes smaller, V_{Rc} becomes smaller, which may need an amplification for the defect detectability. This may lead to a greater test cost. Thus, R_c of the test method is specified by using a process variation of MOS transistors.

I_{Dt} of a defect-free IC varies owing to process variation of MOS transistors. The variation of I_{Dt} is defined as a range from I_{Dtnmin} to I_{Dtnmax} in Figure 4.24. When a hard open defect occurs, V_{Rc} becomes zero regardless of the process variation. When a capacitive open defect occurs, V_{Rc} becomes zero, regardless of process variation, by reducing the test speed. Thus, these are detected by this test method regardless of process variation.

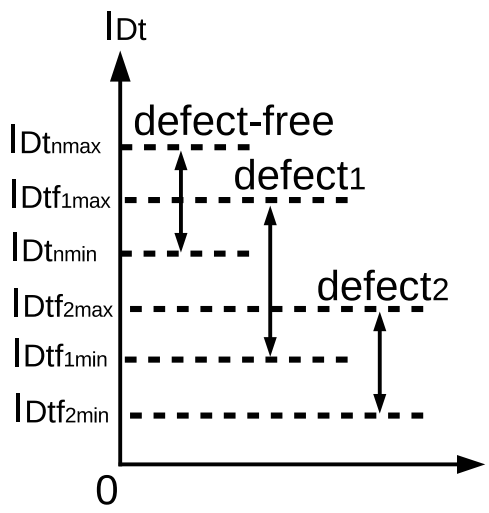


Figure 4.24 Detectable resistive open defect

On the other hand, a dependence on both process variation and the test speed happens in tests attempting to detect resistive open defects. A resistive open defect of large resistance causes a logical error. Thus, the defect is easily detected by measuring logic values. However, resistive open defects of small resistance cannot be detected by measuring logic values, because the defect generates timing errors. These should be detected by the test method advocated in this paper. V_{Rc} appears momentarily whenever an open defect occurs at an interconnect. It is because I_{Dt} flows whenever an H level signal is provided to the interconnect and stops flowing whenever an L level signal is provided to the interconnect. Thus, it depends only on process variation whether a resistive open defect can be detected. The minimum resistance R_{fmin} of resistive open defects that can be detected by the test method is derived from the process variation of MOS transistors.

I_{Dt} of a defective IC varies as in I_{Dt} of defect-free ICs. I_{Dt} of a defective IC that includes a resistive open defect of $defect1$ varies in a range from $I_{Dtf1min}$ to $I_{Dtf1max}$, which is defined in Figure 4.24. The defect is not detected by the test method, because I_{Dt} of the defective IC can be greater than I_{Dtnmin} owing to the process variation. A resistive open defect of $defect2$ will be detected by the test method, because the maximum I_{Dt}, I_{Df2max}, is smaller than I_{Dtnmin}.

Process variations of MOS transistors are modeled as the following four worst-case design corners [39]: (Fast-Fast), (Fast-Slow), (Slow-Fast) and (Slow-Slow) for a pair of nMOS and pMOS. Thus, the range of I_{Dt} of the defective circuit in which R_f is inserted in $S1$ in Figure 4.8 was derived under the process variations by SPICE simulation. R_f from the simulation results was derived so that the maximum I_{Dt} can be smaller than I_{Dtnmin}. Because the testability of resistive open defects may depend on R_c, the minimum resistive open defect, this study examines R_{fmin}, for $R_c = 0\Omega$, 100Ω, 300Ω and 600Ω.

Table 4.1 shows the resistive open defects detected by the test method when $R_c = 0\Omega$, 100Ω, 300Ω and 600Ω. As shown in Table 4.1, R_{fmin} depends on R_c, as is apparent from Figure 4.23. The table also shows that resistive open defects whose resistance is 750Ω or more are detected by the test method under the process variation when $R_c = 300\Omega$. The resistive open defect of $R_f = 750\Omega$ generates an additional propagation delay of 279 psec as shown in Figure 4.14. Thus, open defects causing a propagation delay time of 279 psec or more are detected by our test method under the process variation.

Table 4.1 Detectable resistive open defects

R_c [Ω]	Defect-free circuit [mA]		R_{fmin} [Ω]
	I_{Dtmin}	I_{Dtmax}	
0	4.36	6.89	420
100	3.14	4.66	530
300	2.05	2.87	750
600	1.38	1.85	1060

This paper discusses the detectability of open defects in 3D stacked ICs of 0.18μm CMOS process. V_{DDIO} for dies of an ultra-deep submicron CMOS process is smaller. As the voltage of V_{DDIO} decreases, V_{Rc} becomes smaller than 3.3V. Thus, an amplifier should be used to amplify V_{Rc} in tests to make it easy to be measured. However, open defects can be detected by means of the amplified V_{Rc}, because I_{Dt} change will be caused in such an ultra-deep submicron IC by open defects.

4.4.2 Effectiveness of a revised built-in test circuit

The built-in test circuit proposed in this chapter is a revised version of the one proposed in [37]. In this section, it is compared with the one proposed in [37].

Pin overhead of the revised test circuit is the same as [37], because only one Tst terminal should be added to each die. In the revised test circuit, a couple of an nMOS switch and a diode are added to each input terminal of a die. The diode is made of a MOS. Thus, area overhead of the test circuit is $2N_i$, where N_i is the number of input interconnects of the die. Because it is smaller than the number of MOSs in the core circuits implemented inside dies, the area overhead will be accepted in a real design.

On the other hand, ΔI_{Dt} caused by a resistive open defect that can be detected by the test circuit is larger than [37]. Whenever an interconnect b is tested by the test circuit of [37], I_{Dt2} does not flow through R_c as shown in Figure 4.4. Therefore, ΔV_{Rc} become small regardless of I_{Dt} changes owing to a resistive open defect. The equivalent circuit of test circuit in [37] is shown in Figure 4.25. When $Tst_2 = H$, a circuit block CBx is modeled as a resistor that is made of an nMOS switch connected to b, R_c and a circuit block CBy. CBy is made of nMOS switches connected to R_c, and output buffer gates inside $Die\#1$ that are connected to the nMOS switches. In the equivalent circuit, R_p and R_i in Figure 4.21(a) are omitted, because the resistances are very small.

When $Tst_2 = H$, CBx and CBy are modeled as resistors. Thus, I_{Dt} is specified by an $I_{Dt} - V_{DS}$ characteristic curve of a pMOS connected to b. When it is a defect-free IC, I_{Dt} flows that is expressed by (4.9).

$$\mathrm{I_{Dt}} = \frac{V_{DDIO} - V_{DSp}}{R_{CBx}} \tag{4.9}$$

where R_{CBx} is an equivalent resistance of CBx, and V_{DSp} is the voltage across the drain and the source terminals of $Mp1$. Hence, I_{Dt} specified by $P1$ in Figure 4.26 flow in the defect-free IC.

When a resistive open defect of R_f occurs at b, I_{Dt} flows that is expressed by

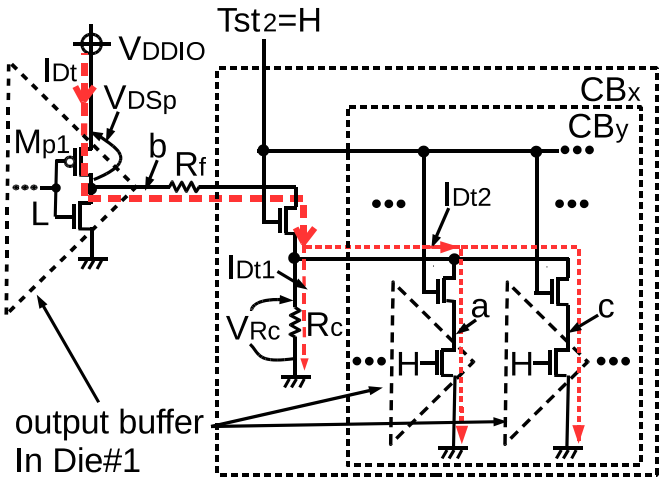


Figure 4.25 Equivalent circuit in a test of b in Figure 4.4

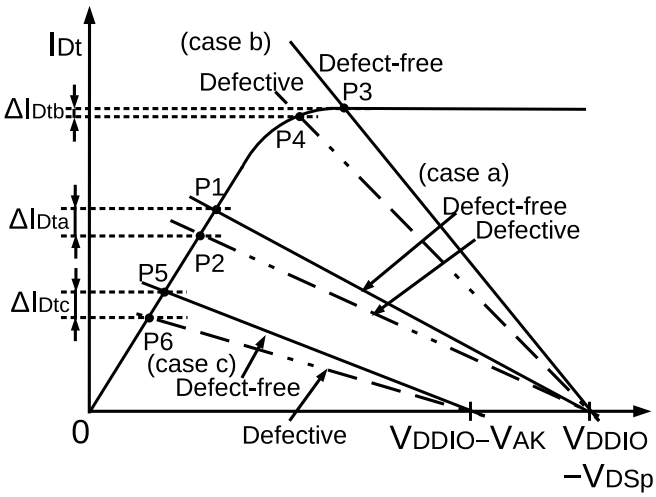


Figure 4.26 ΔI_{Dt} caused by a resistive open defect

(4.10).

$$\mathrm{I_{Dt}} = \frac{V_{DDIO} - V_{DSp}}{R_{CBx} + R_f} \tag{4.10}$$

Thus, I_{Dt} specified by $P2$ in Figure 4.26, flows in the defective IC, and ΔI_{Dta} appears.

As the number of interconnects between $Die\#1$ and $Die\#2$ increases, the resistance of CBy becomes small, and finally the pMOS operates in the saturation mode. Thus, the equivalent resistance of CBx becomes small and I_{Dt} specified by

$P3$ flows when it is a defect-free IC. When a resistive open defect occurs at b, I_{Dt} specified by $P4$ flows as in $P1$ and $P2$. Because ΔI_{Dtb} is smaller than ΔI_{Dta}, as shown in Figure 4.26, ΔV_{Dt} becomes small as the number of interconnects between them increases. On the other hand, I_{Dt} specified by $P5$ flows into the circuit shown in Figure 4.21(a), because the voltage across the diode is a forward voltage, V_{AK}, independent of I_{Dt} when I_{Dt} flows. When a resistive open defect of R_f occurs at b, I_{Dt} specified by $P6$ flows, and ΔI_{Dtc} appears. The I_{Dt} is specified from Figure 4.23. Thus, ΔI_{Dtc} is independent of the number of interconnects between dies in the case of the testable designed dies shown in Figure 4.6(a).

When the number of interconnects between them is small, ΔI_{Dta} may be larger than ΔI_{Dtc}, as shown in Figure 4.26. However, there are a huge number of interconnects between dies in a 3D stacked IC. In this case, ΔI_{Dt} and ΔV_{Rc} in [37] become smaller than the ones in the circuit made of the testable designed dies in Figure 4.6(a). Thus, resistive open defects of smaller resistance are detected by the test circuit proposed in this paper than [37].

To examine it, the sensitivity of resistive open defects by the circuit proposed in this paper was examined by SPICE simulation. Layouts of $Die\#2$ in Figure 4.8 were designed, whose number of input interconnects are 4, 8, and 16, and replaced the diodes in CBb to metal lines. Then, they were converted to SPICE netlists with $Virtuoso$ by Cadence. SPICE netlists were coded to the simulation circuits in Figure 4.8 made of the designed dies. A resistive open defect was inserted in the netlists by adding R_f of 750Ω to $S1$. ΔI_{Dt} and ΔV_{Rc} were derived with $R_c = 300\Omega$ when $Tst_2 = H$ by SPICE simulation. The simulation results are summarized in Table 4.2.

As shown in Table 4.2, both ΔI_{Dt} and ΔV_{Rc} in the test method proposed in [37] become small as the number of the input interconnects increases. Also, ΔV_{Rc} of the circuit made of eight interconnects is smaller than 158.4mV.

The number of interconnects between dies is large in a real 3D stacked IC. Thus, sensitivity of resistive open defects in the test method is higher than [37].

In case of capacitive open defects and hard open defects, I_{Dt} will not flow in the

Table 4.2 ΔI_{Dt} and ΔV_{Rc} of the revised test circuit and the previous test circuit [37]

n	Revised test circuit		Previous test circuit [37]	
	ΔI_{Dt} [mA]	ΔV_{Rc} [mV]	ΔI_{Dt} [mA]	ΔV_{Rc} [mV]
4			0.725	217.3
8	0.527	158.4	0.312	93.48
16			0.146	33.96

defective circuits. Thus, sensitivity of the open defects in the test method is the same as the one in [37].

An operating speed of 3D stacked ICs made of dies designed by the test circuit is the same as the one in [37], because an L level signal is provided to Tst terminals of all dies in them.

Both test methods are based on quiescent I_{Dt}. The time for quiescent I_{Dt} to appear after providing a test input vector depends on parasitic parameters (C_p and R_p) of interconnects to which I_{Dt} flows besides R_c and drivability of output buffer gates in dies. All of the C_ps should be charged through R_p. In the case of the test method in [37], the total capacitance made of C_ps depends on the number of interconnects through which I_{Dt} flows. Because there are many interconnects among dies, it takes longer for quiescent I_{Dt} to appear than the test method. The number of test input vectors is the same as [37], because only one input interconnect of a die is tested at a time as in [37]. Thus, test time is able to be shortened by the test method.

I_{Dt} flows in tests of ICs designed by the test circuit is smaller than the one in [37], as shown in Figure 4.26. Thus, ICs will be tested with a lower test power consumption than [37].

I_{Dt} in [37] depends on the number of interconnects between dies. Thus, threshold values of V_{th} should be prepared for each die before the test by considering a process variation. However, V_{th} of the test method is specified only by considering process variation of MOS transistors because of the undependability of I_{Dt} to the number

of interconnects between dies. Hence, the V_{th} preparation is simpler than [37].

On the other hand, the test method proposed in [42] may be based on a quiescent supply current that is made to flow to an interconnect under test, which might be similar to the test method proposed in this paper. However, the test method proposed in this paper may detect and locate a resistive open defect smaller than [42]. Also, an area overhead of the test circuit proposed in this paper is smaller than [42].

4.5 Summary

A built-in test circuit and an electrical test method have been proposed in this chapter. They are for detecting and locating open defects occurring at interconnects between dies in which boundary scan flip flops are embedded. The test method is a revised one proposed in [37].

Testability of the test method is evaluated by SPICE simulations and by some experiments. The simulation results show that an open defect that is modeled as a delay fault generating an additional delay time of 279 psec, and an open defect that generates no logical errors are detected by the test method at a test speed of 200 MHz. Open defects inserted in a PCB circuit are also detected by the test method at a test speed of 1 MHz in the experimental evaluations.

The testability of open defects by the test method is compared with [37]. It is concluded from the simulation results that the test method is more effective than the one proposed in [37]. The area overhead of the test circuit is small and in order of the number of input interconnects of dies in 3D stacked ICs.

Chapter 5 Built-in Electrical Interconnect Test Circuit Not Using Boundary Scan Flip Flops

In Chapter 4, a built-in test circuit was proposed for electrical interconnect tests in which boundary scan flip flops inside each die in a 3D stacked IC were used to provide test input vectors. Boundary scan flip flops are not always embedded inside dies in a 3D stacked IC, such as in ICs used for some consumer electronics. It is therefore impossible to detect an open defect occurring at interconnects between dies using a test method requiring test circuits.

A built-in test circuit is proposed in this chapter for interconnect tests of a 3D stacked IC made of dies without boundary scan flip flops [57] - [59]. A high impedance signal can be outputted to interconnects between dies in 3D stacked ICs. In many cases, either an H or an L level signal is outputted, and this chapter discusses how to test interconnects between dies, to which either an H or an L level signal is outputted in tests.

Sections 5.1 and 5.2 present the built-in test circuit and the electrical interconnect test method, respectively. The experimental results of a testability examination for open defects are presented in Section 5.3. Section 5.4 describes the testability examination results for simulations of this test method.

5.1 Built-in quiescent supply current test circuit

The electrical interconnect test method described in this chapter is based on a measured quiescent supply current made to flow only through the interconnect under test. The built-in test circuit proposed in this chapter is shown as circuit block CBc in Figure 5.1. It is made of pMOS and nMOS switches that are added to any output terminal of the protection circuit for each input interconnect in the dies as shown in Figure 5.1. The source terminals of the pMOS and nMOS switches are connected to a T_{SOP_P} and T_{SOP_N} terminal of the IC, respectively.

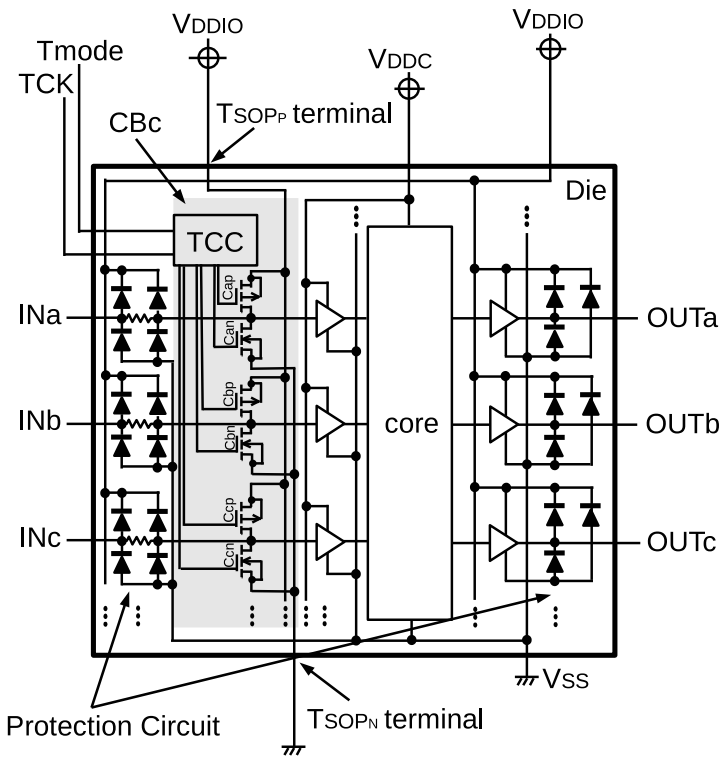


Figure 5.1 Built-in test circuit

The MOS switches are controlled by a test control circuit, TCC, which is connected to the gate terminals of the added MOS switches. The operation of the TCC is shown in Figure 5.2. It works with a test clock signal, TCK, synchronized when an H level signal is provided to a test mode terminal, T_{mode}. Whenever an L level signal is provided to the T_{mode}, the IC works normally.

The output signals of the TCC turn on only either the pMOS or nMOS in the switch circuit connected to the targeted interconnect and turn off the pMOS and nMOS switches in the switch circuit connecting to interconnects other than the targeted one.

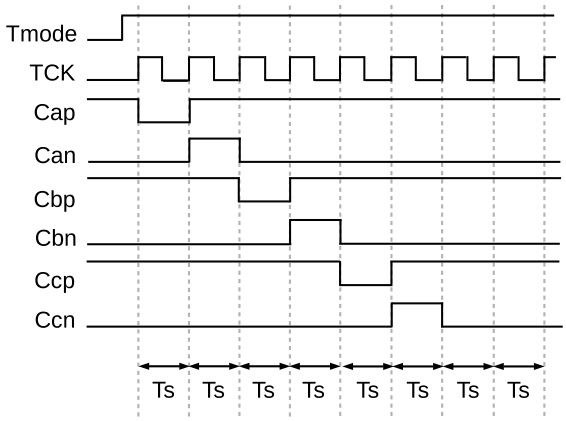
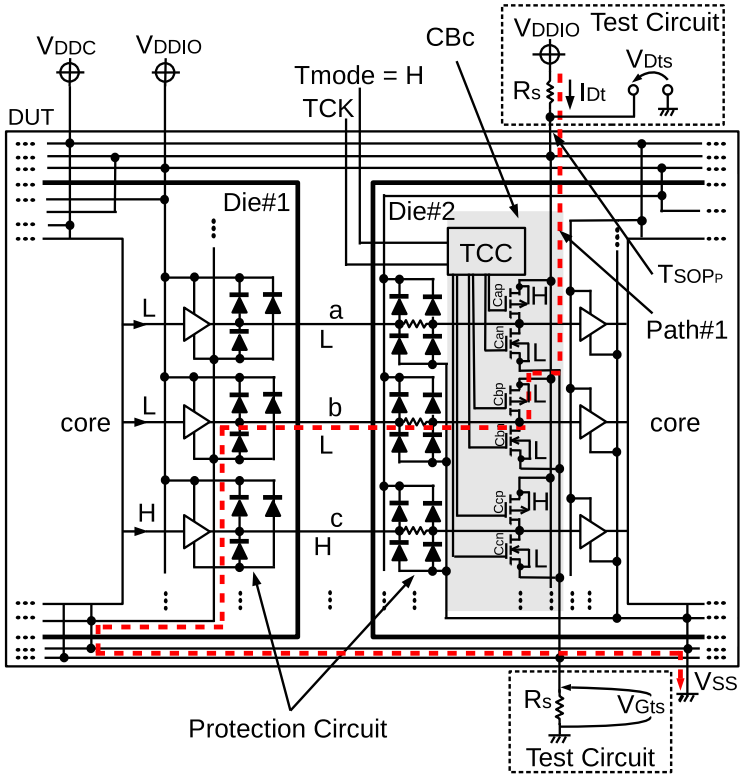


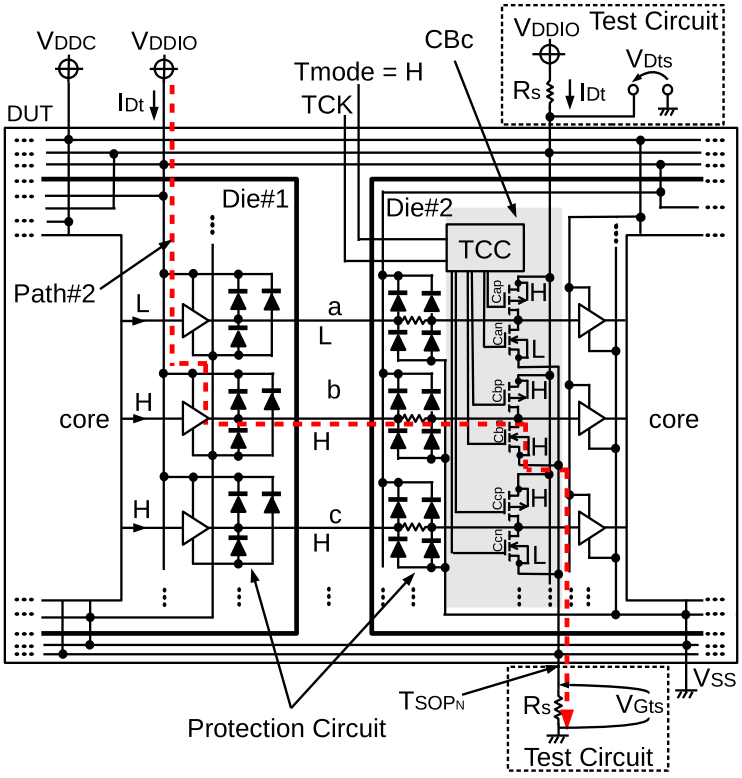
Figure 5.2 Output signals from the TCC

Figure 5.3 shows the principle of the electrical interconnect test method with a built-in test circuit. Interconnects between $Die\#1$ and $Die\#2$ are tested in Figure 5.3. Gate terminals for both the pMOSs and the nMOSs are connected to the TCC. The drain terminals of the pMOS switches are connected to a T_{SOP_P} terminal, while the source terminals of the nMOS switches are connected to a T_{SOP_N} terminal. Whenever an IC made of dies containing the built-in test circuit is tested, a test resistor, R_s, is connected to both the T_{SOP_P} and the T_{SOP_N} terminals, as shown in Figure 5.3.

An interconnect is tested by measuring a quiescent supply current, I_{Dt}, that is made to flow to a targeted interconnect, as in the electrical interconnect test method proposed in Chapter 4. The targeted interconnect in Figure 5.3 is interconnect b. By the TCC, I_{Dt} flows along the current paths, $Path\#1$ and $Path\#2$, as shown in Figure 5.3. Either a quiescent voltage of V_{Dts} or V_{Gts} is measured instead of I_{Dt}.



(a) L outputted from *Die*#1



(b) H outputted from *Die*#1

Figure 5.3 Electrical interconnect test with built-in test circuit

Whenever an L level signal is provided to b, control signals of $Cbp = Cbn = L$ from TCC are provided only to the switch circuit connecting to b. By the control signals, I_{Dt} flows along $Path\#1$ in Figure 5.3(a). V_{Dts} is measured to detect any open defect at b.

The change in I_{Dt} can be measured by V_{Dts}, since V_{Dts} is defined by (5.2). If a hard or capacitive open defect occurs at b, I_{Dt} will not flow, resulting in V_{Dts} being equal to V_{DDIO}. If a resistive open defect occurs at b, I_{Dt} smaller than the defect-free ICs will flow and as a result V_{Dts} will be larger than the defect-free ICs, so if (5.1) is satisfied, an open defect occurs at b.

$$\mathrm{V_{Dts}} - \mathrm{V_{Dtn}} \geq \mathrm{V_{Dth}} \tag{5.1}$$

where V_{Dts} is defined by (5.2). V_{Dtn} is V_{Dts} of the defect-free ICs, and V_{Dth} is a threshold value specified from the variations of V_{Dtn}.

$$\mathrm{V_{Dts}} = \mathrm{V_{DDIO}} - \mathrm{R_s} \cdot \mathrm{I_{Dt}} \tag{5.2}$$

On the other hand, whenever an H level signal is provided to b, control signals of $Cbp = Cbn = H$ from TCC are provided only to the switch circuit connecting to b. By the control signals, I_{Dt} flows along $Path\#2$ in Figure 5.3(b). V_{Gts} is measured to detect an open defect at b.

The change in I_{Dt} can be measured by V_{Gts}, since V_{Gts} is defined by (5.4). If a hard or capacitive open defect occurs at b, I_{Dt} will not flow, resulting in V_{Gts} equaling 0 V. If a resistive open defect occurs at b, I_{Dt} smaller than the defect-free ICs will flow, resulting in a V_{Gts} smaller than defect-free ICs, so if (5.3) is satisfied, an open defect occurs at b.

$$\mathrm{V_{Gtn}} - \mathrm{V_{Gts}} \geq \mathrm{V_{Gth}} \tag{5.3}$$

where V_{Gts} is defined by (5.4). V_{Gtn} is the V_{Gts} of the defect-free ICs, and V_{Gth} is a threshold value specified from variations of V_{Gtn}.

$$\mathrm{V_{Gts}} = \mathrm{R_s} \cdot \mathrm{I_{Dt}} \tag{5.4}$$

It is not specified whether an L or H level signal is provided to interconnects between dies inside DUTs, since boundary scan flip flops are not embedded in the dies. Both $Cbp = Cbn = L$ and $Cbp = Cbn = H$ are provided to the switch circuit in the electrical interconnect test. When $Cbp = Cbn = L$, if an H level signal is provided to b, I_{Dt} is not flowing and b is judged to be a defective interconnect. Similarly, when $Cbp = Cbn = H$, if an L level signal is provided to b, I_{Dt} is not flowing and b is judged to be a defective interconnect.

However, if I_{Dt} flows through b in neither $Cbp = Cbn = L$ nor $Cbp = Cbn = H$, b is defect-free. If an open defect occurs at b, however, it is judged to be defective in both cases, so if both (5.1) and (5.3) are satisfied, an open defect occurs at b.

Interconnect b in Figure 5.3 is tested by the following procedures:

(1) Provide L and H level signals to the T_{mode} terminals of TCC in $Die\#1$ and $Die\#2$, respectively.

(2) Provide a test clock signal, TCK, to TCC per Ts.

(3) Provide an L or H level signal to an interconnect between $Die\#1$ and $Die\#2$.

(4) Turn on one of the MOSs switches in CBc sequentially with the TCC.

(5) Measure both V_{Dts} and V_{Gts} at T_{SOP_P} and T_{SOP_N} terminals, respectively, in the test circuit.

(6) Examine whether (5.1) and (5.3) are satisfied. If both are satisfied, an open defect occurs at b.

5.2 Evaluation of the built-in test circuit

5.2.1 Experimental testability examination

The layout for a die containing CBc was designed with the 0.18μm CMOS technology process of Rohm Co., Ltd. An inverter chain circuit of 16 stages is the core circuit in the die. Figure 5.4 shows the layout of the prototype IC used in experiments. Input and output protection circuits used in the designed die were from the CMOS cell library distributed by VDEC in the University of Tokyo, Japan. However, when the ICs were prototyped by Rohm Co., Ltd., the input and output protection circuits in the designed die were replaced by protection circuits from the IC foundry.

The feasibility of the built-in test circuit for detecting open defects was evaluated experimentally. An experimental circuit with the prototype IC was built and is shown in Figure 5.5. The two source voltages provided to the circuit were specified by the CMOS process: $V_{DDIO} = 3.3$ V, $V_{DDC} = 1.8$ V.

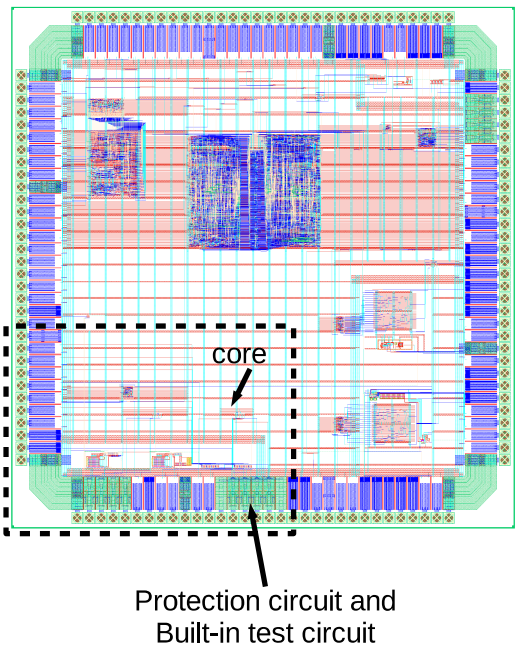


Figure 5.4 Layout of the prototype IC

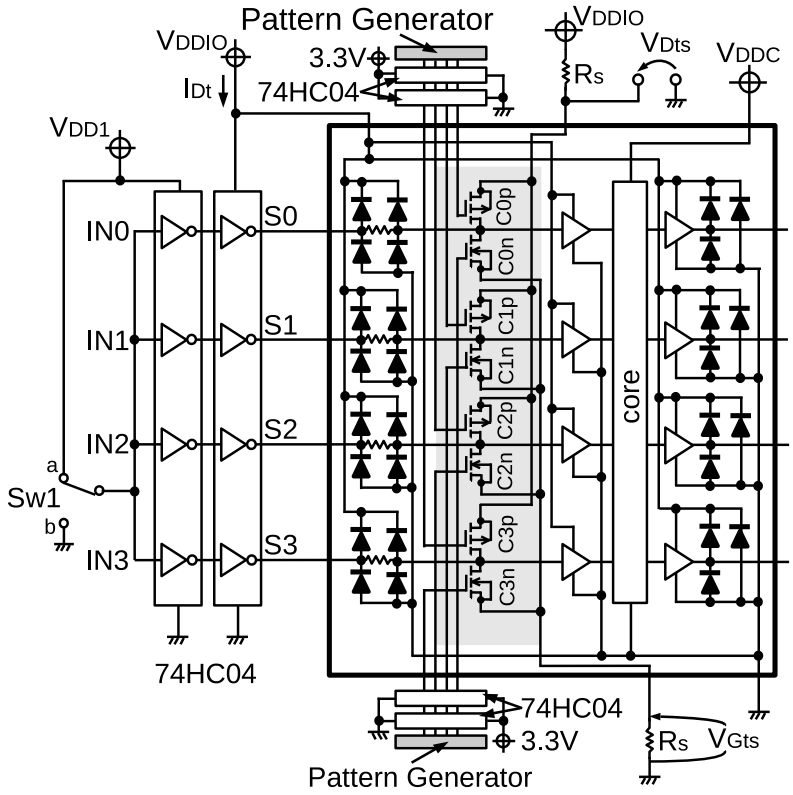


Figure 5.5 Experimental circuit with the prototype IC

Either an L or H level signal was provided to $IN0$, $IN1$, $IN2$ and $IN3$ by a switch, $Sw1$, as shown in Figure 5.5. A resistor of 100 Ω was used as R_s. A hard open defect at $S1$ was inserted by eliminating the connecting wire from 74HC04 of $S1$ in the defect-free circuit. A resistive open defect at $S1$ was inserted by adding a resistor, R_f of 200 Ω to the defect-free circuit. The sizes of the pMOS and nMOS switches in the designed CBc were l = 300 nm, w = 140 μm for the pMOS switch and l = 360 nm and w = 56 μm for the nMOS switch.

The switch control signals for the MOS switches in the test circuit are shown in Figure 5.6. L and H level signals were provided to the circuit per Ts of 1 μsec in the experiment, so that one of the MOS switches could be turned on at a time. V_{Dts} and V_{Gts} were observed by a Tektronix DPO3014 digital oscilloscope.

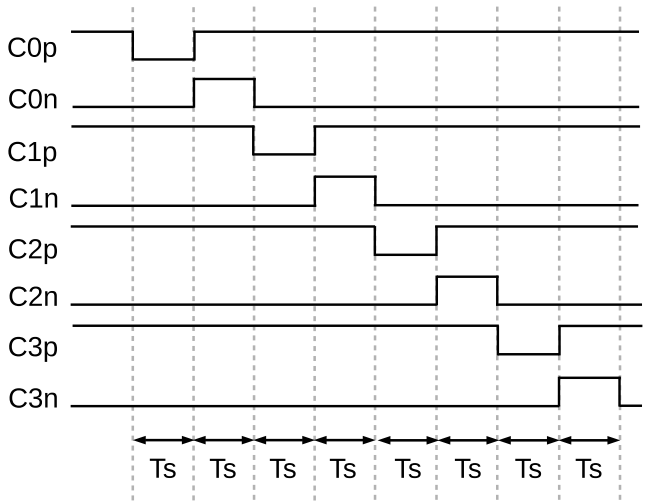


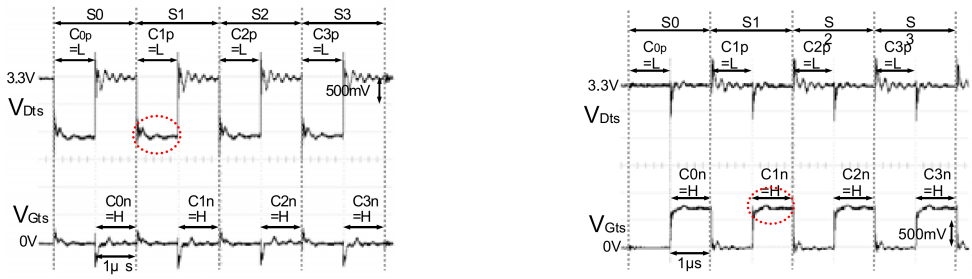
Figure 5.6 Switch control signals for a testable circuit in the prototype IC

The experimental results of the defect-free and three defective circuits when L and H level signals are outputted are shown in Figures 5.7, 5.8, and 5.9; the faulty effects caused by open defects are encircled with a broken line.

V_{Dts} waveforms of the defect-free circuit are shown in Figure 5.7. When an L level signal is provided to interconnects $S0$, $S1$, $S2$ and $S3$, V_{Dts} = 2.2 V and V_{Gts} = 0 V in Figure 5.7(a). When an H level signal is provided, V_{Dts} = 3.3 V and V_{Gts} = 750 mV in Figure 5.7(b).

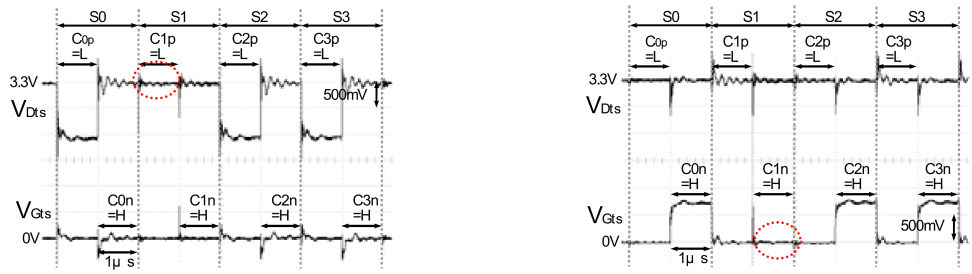
When a hard open defect occurs at $S1$, I_{Dt} does not flow through $S1$ when $C1p = L$ and $C1n = H$. Thus, V_{Dts} and V_{Gts} increase to 3.3 V and decreased to 0 V in Figure 5.8(a) and (b), respectively.

When a resistive open defect of R_f = 200 Ω occurs at $S1$, V_{Dts} is increased by about 500 mV from the defect-free circuit when $C1p = L$ in Figure 5.9(a). When $C1n = H$ in Figure 5.9(b), V_{Gts} is decreased by 500 mV from the defect-free circuit. The hard and resistive open defects are detected by the test method, since both (5.1) and (5.3) are satisfied.



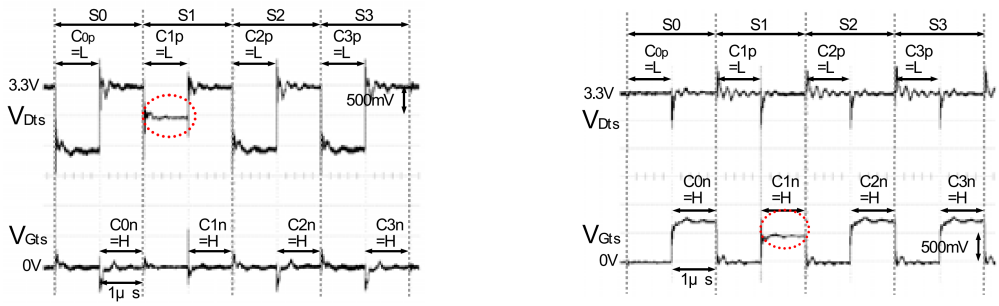
(a) L outputted (b) H outputted

Figure 5.7 Defect-free circuit ($R_f = 0\ \Omega$) at $Ts = 1\ \mu$sec



(a) L outputted (b) H outputted

Figure 5.8 Hard open defect ($R_f = 1$ TΩ) at $Ts = 1\ \mu$sec



(a) L outputted (b) H outputted

Figure 5.9 Resistive open defect of $R_f = 200\ \Omega$ at $S1$ at $Ts = 1\ \mu$sec

5.2.2 Testability examination by simulation

The layout of a die containing CBc was designed using the 0.18μm CMOS technology process of Rohm Co., Ltd., to examine the testability for open defects using the test method. SPICE simulations are used to determine whether open defects occurring at an interconnect between two dies in Figure 5.3 are detected by the test method described in Section 5.1.

A SPICE netlist was extracted from the designed layout depicted in Figure 5.10 with the extraction tool *Virtuoso* produced by Cadence. The simulation circuit shown in Figure 5.11 was coded with the SPICE netlist by adding a parasitic resistor R_p of 2 mΩ and a parasitic capacitor C_p of 242 fF to each interconnect, as shown in Figure 5.11. V_{DDIO}, V_{DDC}, and R_s in the simulations were 3.3 V, 1.8 V and 100 Ω, respectively, which were the same as those used in the experiments described in 5.2.1.

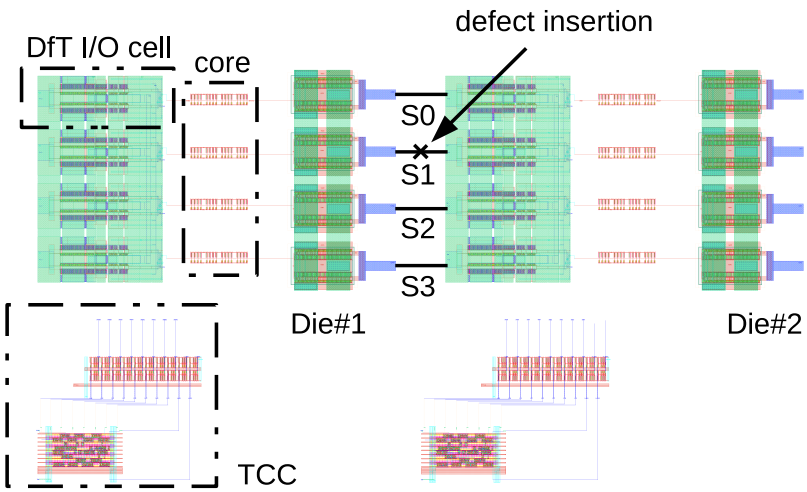


Figure 5.10 Layout extracted from the designed die

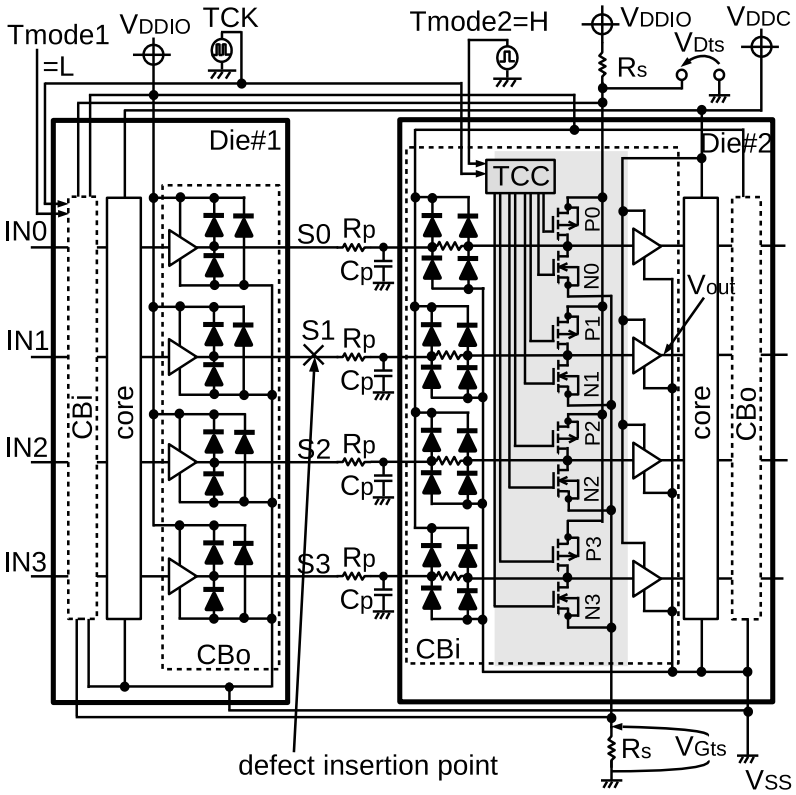


Figure 5.11 Simulation circuit

A hard open defect was inserted into interconnect $S1$ by adding a resistor R_f of 1 TΩ to the coded netlist to examine whether a hard open defect was detectable. A resistive and a capacitive open defect were inserted into $S1$ and $S2$ by adding a resistor R_f and a capacitor C_f to the netlist, respectively.

The switch control signal of the MOS switches in the simulations is shown in Figure 5.12. L and H level signals were provided from the TCC to the circuit per Ts of 1 μsec and 0.5 μsec in the simulation to make one of the switches turn on at a time.

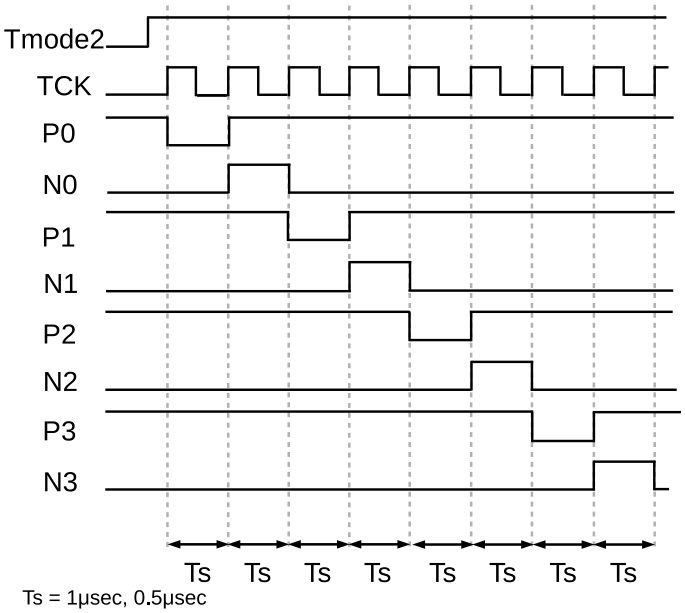


Figure 5.12 Switch control signals

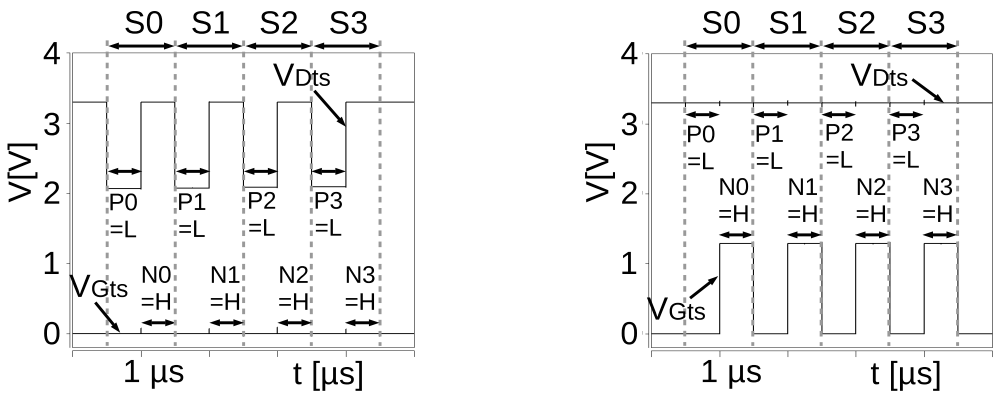
The simulation results of V_{Dts} and V_{Gts} waveforms of the defect-free and three defective circuits when an L or an H level signal is outputted to the interconnects are shown in Figures 5.13, 5.14, 5.15, 5.16, and 5.17, where the faulty effects caused by open defects are encircled by a broken line.

When an L level signal is provided to interconnects $S0$, $S1$, $S2$, and $S3$ in the defect-free circuit, $V_{Dts} = 2.07$ V and $V_{Gts} = 0$ V, as shown in Figure 5.13(a). When an H level signal is provided to them, $V_{Gts} = 1.29$ V and $V_{Dts} = 3.3$ V, as shown in Figure 5.13(b).

When a hard open defect occurs at $S1$, $V_{Dts} = 3.3$ V in Figure 5.14(a). The V_{Dts} is larger than the 2.07 V when $P1 = L$ in Figure 5.14(a). When $N1 = H$ in Figure 5.14(b), $V_{Gts} = 0$ V. The V_{Gts} in Figure 5.14(b) is smaller than 1.29 V.

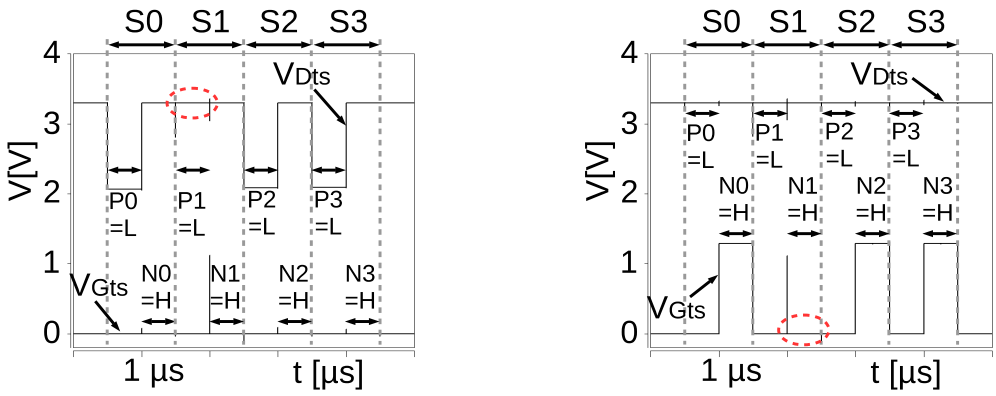
R_f of 100 Ω, 150 Ω, and 200 Ω are inserted into $S1$ to identify the minimum resistive open defect detectable using the test method [58]. In Figure 5.15, R_f of 150 Ω is recognized as the minimum resistive open defect. The voltage differences from the defect-free circuit in Figure 5.13 are 0.20 V and 0.22 V when $P1 = L$ and $N1 = H$, respectively. When R_f of 100 Ω is inserted into $S1$, V_{Dts} and V_{Gts} are approximately equal to the defect-free circuit, so based on Figure 5.15, resistive

open defects of $R_f \geq 150\ \Omega$ can be detected at a test speed of 500 kHz, since each interconnect is tested per 2 μsec in the simulation.



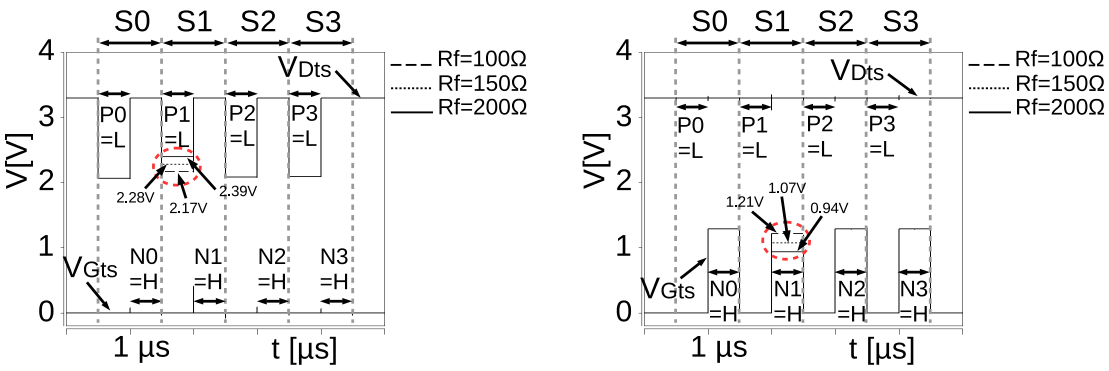
(a) L outputted (b) H outputted

Figure 5.13 Defect-free circuit ($R_f = 0\ \Omega$) at $Ts = 1\ \mu$sec



(a) L outputted (b) H outputted

Figure 5.14 Hard open defect ($R_f = 1$ TΩ) at $Ts = 1\ \mu$sec



(a) L outputted (b) H outputted

Figure 5.15 Test of resistive open defect at $Ts = 1$ μsec

During the stacking of KGDs in 3D stacked ICs, mechanical stress is applied to the KGDs, which can result in a capacitive open defect in a TSV. A capacitive open defect can be illustrated as a crack in the TSV, as shown in Figure 5.16. The crack in the TSV is filled with air. The capacitance of a capacitive open defect, C_f, is calculated by the formula of a parallel plate capacitor and is expressed by (5.5).

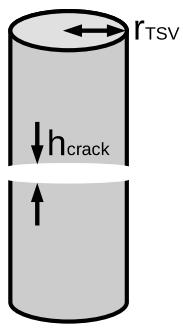


Figure 5.16 A single crack in a TSV

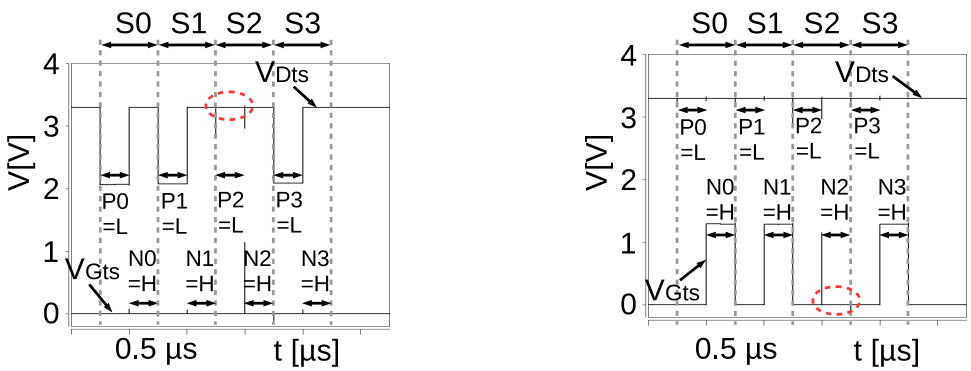
$$\mathrm{C_f} = \xi_{air}\xi_0\frac{r_{TSV}^2}{h_{crack}} \tag{5.5}$$

where ξ_{air} is the relative permittivity of air, ξ_0 is the permittivity of vacuum, h_{crack} is the crack height, and r is the radius of the TSV.

SPICE simulations were used to examine whether a capacitive open defect occurring at interconnects between two dies in Figure 5.11 was detectable. The capacitive

open defect of the cracked structure, h_{crack} was simulated for 1 nm, 10 nm, 100 nm and 1 μm. Capacitors, C_f, corresponding to the h_{crack} were inserted into $S2$ [59].

Figure 5.17 show the V_{Dts} and V_{Gts} waveforms for the defective circuits. The same V_{Dts} and V_{Gts} waveforms appear when capacitive open defects, C_f, corresponding to the h_{crack} of 1 nm, 10 nm, 100 nm and 1 μm occur at $S2$, as shown in Figure 5.17. I_{Dt} from V_{DDIO} flows through $S2$ when $P2 = L$ and $N2 = H$ so as to charge C_f. As C_f charges, I_{Dt} decreases and V_{Dts} and V_{Gts} begin to increase and decrease, respectively. When C_f is fully charged, I_{Dt} stops flowing and V_{Dts} and V_{Gts} become 3.3 V and 0 V, respectively at a test speed of 1 MHz.



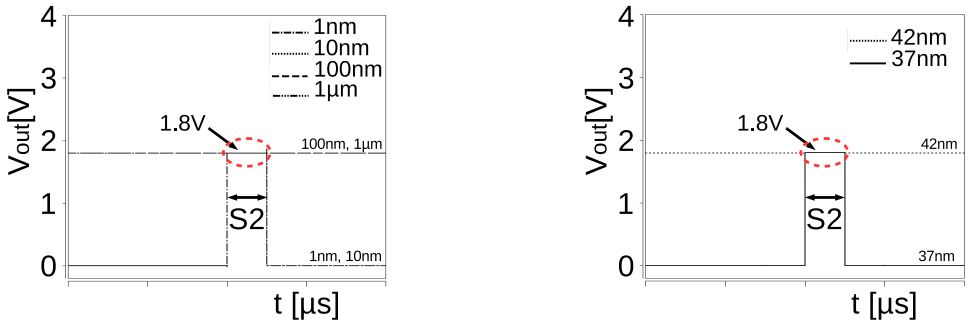
(a) L outputted (b) H outputted

Figure 5.17 Tests for capacitive open defects at $Ts = 0.5$ μsec

A high speed logic signal can be propagated through a capacitive open defect. Voltage waveforms at V_{out} in the simulation circuit with $T_{mode_2} = L$ are shown in Figure 5.18. Figure 5.18(a) shows the V_{out} waveforms for h_{crack} of 1 nm, 10 nm, 100 nm and 1 μm. An H level signal propagates to V_{out} when $h_{crack} \leq 10$ nm. However, an H level signal does not propagate to V_{out} when $h_{crack} \geq 100$ nm.

An H level signal can also be propagated through a capacitive open defect of 10 nm $\leq h_{crack} \leq$ 100 nm. Examinations were carried out to identify the maximum h_{crack} through which an H level signal could be propagated. Figure 5.18(b) shows the V_{out} waveforms for an h_{crack} of 37 nm and 42 nm. In Figure 5.18(b), an H level signal propagates to V_{out} when h_{crack} is 37 nm and does not propagate to V_{out} when h_{crack} is 42 nm. Thus, an H level signal can be propagated through a

capacitive open defect that is 1 nm $\leq h_{crack} \leq$ 37 nm, which means that such defects cannot be detected by measuring logic values, since no logical errors appear. Thus, capacitive open defects undetectable by measuring logic values are detected by this test method.



(a) H outputted (b) H outputted

Figure 5.18 V_{out} at $S2$

The built-in test circuit is made of a pair of pMOS and nMOS switches and a TCC. The area overhead of the test circuit is $18Ni + 4MOSs$, where Ni is the number of input interconnects of the dies. Since it is smaller than the number of MOSs in the core circuits implemented in the dies, the area overhead will be accepted in the actual design.

If open defects occur at more than one interconnect simultaneously, the open defects will be detected by the test method, since only one interconnect is tested at a time.

5.3 Summary

A built-in test circuit and an electrical test method have been proposed in this chapter for detecting and locating open defects at interconnects between dies in which boundary scan flip flops are not embedded.

The testability of the test method was evaluated both by SPICE simulation and experimentally using a prototype IC designed by the test circuit. Open defects inserted into the PCB circuit were detected by the test method in experiments

at a test speed of 500 kHz. Parasitic resistance and parasitic capacitance at an interconnect in a 3D stacked IC are smaller than the PCB circuit, so an open defect in the IC can be detected at test speeds faster than 500 kHz. The simulation results show that open defects with resistance of 150 Ω and above and open defects that generate no logical errors are detected by the test method at a test speed of 1 MHz.

Chapter 6 Conclusions

In this paper, two kinds of built-in quiescent supply current test circuits and electrical interconnect test methods have been proposed for detecting and locating open defects at interconnects between dies in 3D stacked ICs. These are for post-bond testing of 3D stacked ICs. This paper discussed whether open defects are detected at interconnects between dies in a 3D stacked IC using test methods with built-in test circuits.

Such open defects are classified into the following three types: resistive, hard, and capacitive open defects. Such defects, which are the ones to be detected using the test methods, can impede, break down, or cause logical errors in defective ICs. Tests of 3D stacked ICs are therefore indispensable to guarantee a sufficient outgoing product quality to the customer.

Previously, a built-in test circuit and an electrical interconnect test method were proposed by T. Konishi *etal.* using boundary scan flip flops embedded inside the dies [37]. The test method is based on the quiescent supply current of an IC under test. The built-in test circuit is composed of nMOS switches added to the output terminals of the input protection circuits of each input interconnect in the dies. This test circuit is revised in this paper to achieve high sensitivity to quiescent supply current change caused by open defects. In the revised test circuit, a diode is added to each of the source terminals of the nMOS switches. The test circuit was examined by SPICE simulation and experimentally using a PCB circuit made of a prototype IC containing the test circuit to determine whether the test circuit could detect open defects. The simulation results indicated that an open defect modeled as a delay fault generating an additional delay time of 279 psec and an open defect generating no logical errors are detected with the revised test circuit at a test speed of 200 MHz. Open defects inserted into the PCB circuit are also detected with the test circuit at a test speed of at least 1 MHz. SPICE simulations were also used to examine the testability of the test method under a process variation of MOS transistors of the test circuit. The simulation results showed that the revised test circuit could detect

resistive open defects of smaller resistance than the [37].

To reduce the cost of 3D stacked ICs, boundary scan flip flops are sometimes not embedded in the dies. This paper proposed a built-in test circuit and an electrical interconnect test method to test 3D stacked ICs made of dies without boundary scan flip flops. The feasibility of the tests were examined experimentally with a prototype IC designed by the test circuit, as well as through SPICE simulations. The experimental results showed that the test method detected open defects inserted into the PCB circuit at a test speed of 500 kHz. The simulation results showed that the test method detects resistive open defects of 150 Ω and above, as well as capacitive open defect generating no logical errors with a maximum crack height of 37 nm at a test speed of 1 MHz.

Open defects can occur at interconnects between dies in a 3D stacked IC during stacking. Open defects that generate timing errors may not be detected by boundary scan testing. In this paper, it is shown that open defects can be detected using built-in test circuits, which may result in the realization of high-reliability systems made of 3D stacked ICs with the test circuits. The feasibility and testability of the test circuits have been examined, but the test circuits have not been evaluated in a fabricated 3D stacked IC, and such an evaluation remains for a future study.

Bibliography

[1] Our World in Data - Technology, Technological Progress, (online), available from: https://ourworldindata.org/grapher/transistors-per-microprocessor, (accessed on June 18, 2018)

[2] J. D. Meindl, Q. Chen and J. A. Davis, “Limits on Silicon Nanoelectronics for Terascale Integration”, Science, Vol. 293, No. 5537, pp. 2044-2049, 2001

[3] International Technology Roadmap for Semiconductors 2009 Edition - Interconnect, (online), available from: https://www.semiconductors.org/clientuploads/Research_Technology/ITRS/2-009/Interconnect.pdf, (accessed on June 18, 2018)

[4] K. Bernstein, et al., ”Interconnects in the third dimension: design challenges for 3D ICs”, Proc. Design Automation Conf., pp. 562-567, 2007

[5] V. F. Pavlidis and E. G. Friedman, ”Three-dimensional Integrated Circuit Design”, Morgan Kaufman, 2009

[6] Bryan Black, et. al, ”Die Stacking (3D) Microarchitecture”, Proc. 39th International Symposium on Microarchitecture, 2006

[7] P. Garrou, C. Bower and P. Ramm, ”Handbook of 3D Integration”, Weinheim, Germany: Wiley, 2008

[8] E. J. Marinissen, ”Testing TSV-Based Three-Dimensional Stacked ICs”, Proc. Design, Automation and Test, pp. 1689-1694, 2010

[9] Makoto Motoyoshi, ”Through-Silicon Via (TSV)”, Proc. IEEE, Vol. 97, Issue 1, pp. 43-48, 2009

[10] W. Rhett Davis, John Wilson, Stephen Mick, Jian Xu, Hao Hua, Christopher Mineo, Ambarish M. Sule, Michael Steer and Paul D. Franzon, ”Demystifying 3D ICs: the pros and cons of going vertical”, IEEE Design and Test of Computers, Vol. 22, Issue 6, pp. 498-510, 2005

[11] Hsien-Hsin S. Lee, Krishnendu Chakrabarty, ”Test Challenges for 3D Integrated Circuits”, IEEE Design & Test of Computers, Vol. 26, No. 5, pp. 26-35, 2009

[12] Daniel H. Jung, Joohee Kim, Jonghoon J. Kim, Joungho Kim, Jun So Pak, "Disconnection failure model and analysis of TSV-based 3D ICs", Proc. IEEE Electrical Design of Advanced Packaging and Systems Symposium, pp. 164-167, 2012

[13] C. Metzler, A. Todri, A. Bosio, L. Dilillo, P. Girard, A. Virazel, "Through-Silicon-Via resistive-open defect analysis", Proc. 17th IEEE European Test Symposium, pp. 1, 2012

[14] E. J. Marinissen and Y. Zorian, "Testing 3D Chips Containing Through-Silicon Vias", Proc. IEEE International Test Conf., pp. 1-11, 2009

[15] S. Y. Huang, "Pre-bond and Post-bond Testing of TSVs and Die-to-Die Interconnects", Proc. IEEE Asian Test Symposium, pp. 80-85, 2016

[16] E. J. Marinissen, "Challenges in Testing TSV-Based 3D Stacked ICs: Test Flows, Test Contents, and Test Access", Proc. IEEE Asia Pacific Conf. on Circuits and Systems, pp.544-547, 2010

[17] C. W. Chou, J. F. Li, J. J. Chen, D. M. Kwai, Y. F. Chou and C. W. Wu, "A Test Integration Methodology for 3D Integrated Circuits", Proc. 19th IEEE Asian Test Symposium, pp.377-38, 2010

[18] B. Noia, K. Chakrabarty and E. J. Marinissen, "Optimization Methods for Post-Bond Die-Internal/External Testing in 3D Stacked ICs", Proc. IEEE International Test Conf., pp.1-9, 2010

[19] M. Gulbins, F. Hopsch, P. Schneider, B. Straube and W. Vermeiren, "Developing Digital Test Sequences for Through-Silicon Vias within 3D Structures", Proc. IEEE International 3D Systems Integration Conf., pp.1-6, 2010

[20] Y. J. Huang, J. F. Li, J. J. Chen, D. M. Kwai, Y. F. Chou and C. W. Wu, "A Built-In Self-Test Scheme for the Post-Bond Test of TSVs in 3D ICs", Proc. 29th IEEE VLSI Test Symposium, pp.20-25, 2011

[21] K. Chakrabarty, M. Agrawal, S. Deutsch, B. Noia, R. Wang and F. Ye, "Test and Design-for-Testability Solutions for 3D Integrated Circuits", IPSJ Trans. on System LSI Design Methodology, Vol. 7, pp. 56-73, 2014

[22] M. Aoyagi, et. al, "Developing a leading practical application for 3D IC chip

stacking technology - How to progress from fundamental technology to application technology", Journal of Synthesiology, Vol.9, No.1, p.1-14, 2016.(Translated from Synthesiology)

[23] R. Rashidzadeh, E. Jedari, T. M. Supan and V. Mashkavtsev, "A DLL-Based Test Solution for Through Silicon Via (TSV) in 3D-Stacked ICs", Proc. IEEE International Test Conference, pp. 1-9, 2015

[24] Y. C. Tan, C. M. Tan, X. W. Zhang, T. C. Chai and D. Q. Yu, "Electromigration performance of Through Silicon Via (TSV) - A modeling approach", Journal of Microelectronics Reliability, Vol. 50, Issue 9-11, pp. 1336-1340, 2010

[25] J. W. You, S. Y. Huang, D. M. Kwai, Y. F. Chou, C. W. Wu, "Performance Characterization of TSV in 3D IC via Sensitivity Analysis", Proc. IEEE 19th Asian Test Symposium, pp.389-394, 2010

[26] M. Benabdeladhim, B. Hamdi and A. Fradi, "Based IBIST auto-parallel reconfiguration of TSV defect in 3D-IC", Proc. 2nd World Symposium on Web Applications and Networking (WSWAN), pp.1-6, 2015

[27] D. Malta, et. al, "Characterization of thermo-mechanical stress and reliability issues for Cu-filled TSVs", Proc. 61st Electronic Components and Technology Conference, pp.1815-1821, 2011

[28] Wikipedia - Electromigration, (online), available from: https://en.wikipedia.org/wiki/Electromigration, (accessed on June 18, 2018)

[29] H. Ceric, S. Selberherr, "Electromigration in submicron interconnect features of integrated circuits", Journal of Materials Science and Engineering, Vol. 71, Issue 5-6, pp. 53-86, 2011

[30] J. Lienig, "Electromigration and Its Impact on Physical Design in Future Technologies", Proc. ACM International Symposium on Physical Design, pp. 33-40, 2013

[31] J. R. Black, "Electromigration - A brief survey and some recent results", IEEE Trans. on Electronic Devices, Vol. 16, Issue 4, pp. 338-347, 1969

[32] G. Van der Plas, et.al, "Design Issues and Considerations for Low-Cost 3-D

TSV IC Technology", IEEE Journal of Solid-State Circuit, Vol. 46, Issue 1, pp. 293-307, 2010

[33] X. Gao, R. Chen, X. Wang, X. Luo and S. Liu, "Thermo-mechanical reliability of copper-filled and polymer-filled through silicon vias in 3D interconnects", Proc. 63rd IEEE Electronic Components and Technology, pp. 2132-2137, 2013

[34] M. Hashizume, S. Kondo and H. Yotsuyanagi, "Possibility of Logical Error Caused by Open Defects in TSVs", Proc. International Technical Conference on Circuits, Computers and Communications, pp.907-910, 2010

[35] T. Konishi, H. Yotsuyanagi and M. Hashizume, "Supply Current Testing of Open Defects at Interconnects in 3D ICs with IEEE 1149.1 Architecture", Proc. IEEE International 3D Systems Integration Conf., pp.8-2-1-8-2-6, 2012

[36] T. Konishi, H. Yotsuyanagi and M. Hashizume, "A Built-in Test Circuit for Supply Current Testing of Open Defects at Interconnects in 3D ICs", Proc. of 4th Electronics System Integration Technologies Conference (ESTC2012), pp.PA21.1_1 - PA21.1_6, 2012

[37] M. Hashizume, T. Konishi and H. Yotsuyanagi, "Electrical Testable Design for Open Defects at Logic Signal Lines between Dies in 3D ICs", Trans. of IEICE, No.J96-C, No.11, pp.361-370, 2013.(In Japanese)

[38] H. Sung, K. Cho, K. Yoon, and S. Kang, "A Delay Test Architecture for TSV With Resistive Open Defects in 3D Stacked Memories", IEEE Trans. on Very Large Scale Integration Systems, Vol. 22, Issue 11, pp. 2380-2387, 2014

[39] N. H. E. Weste and D. M. Harris, "CMOS VLSI Design, Circuits and System Design Fourth Edition", pp.244-246, Addison-Wesley, 2009

[40] E. J. Marinissen, C. C. Chi, J. Verbree and M. Konijnenburg, "3D DfT architecture for pre-bond and post-bond testing", Proc. IEEE International 3D Systems Integration, pp. 1-8, 2010

[41] N. Kandalaft, R. Rashidzadeh and M. Ahmadi, "Testing 3D-IC Through-Silicon-Vias (TSV ' s) by Direct Probing", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 32, Issue 4, pp. 538-546, 2013

[42] F. Ye and K. Chakrabarty, "TSV Open Defects in 3D Integrated Circuits: Characterization, Test, and Optimal Spare Allocation", Proc. of Design Automation Conf., pp. 1024-1030, 2012

[43] S. Y. Huang, J. Y. Lee, K. H. Hans Tsai and W. T. Cheng, "Pulse-Vanishing Test for Interposers Wires in 2.5-D IC", IEEE Trans. on Computer-Aided Design of Electronic Circuits(TCAD), Vol. 33, No. 8, pp. 1258-1268, 2014

[44] S. Y. Huang, K. H. Tsai, W. T. Cheng and J. Y. Lee, "Method and circuit of pulse-vanishing test", Mentor Graphics and A Siemens Business, U.S. Patent 9, 720,038, 2017

[45] V. N. Sekhar, S. Neo, L. H. Yu, A. D. Trigg and C. C. Kuo, "Non-destructive Testing of a High Dense Small Dimension Through Silicon Via (TSV) Array Structures by Using 3D X-ray Computed Tomography Method (CT scan)", Proc. 12th Electronics Packaging Technology Conf., pp.462-466, 2010

[46] S. H. Lau, A. Tkachuk, M. Feser, H. Cui, F. Duewer, W. Yun and D. Vallet, "Non Destructive Failure Analysis Technique With a Laboratory Based 3D X-ray Nanotomography System", Proc. LSI Testing Symposium, 2006

[47] H. Roth, Z. He and T. Mayer, "Inspection of through silicon vias (TSV) and other interconnections in IC packages by computed tomography", Proc. of 3rd Electronics System Integration Technology Conf., pp. 1-4, 2010

[48] L. W. Kong, A. C. Rudack, P. Krueger, E. Zschech, S. Arkalgud, A. C. Diebold, "3D-interconnect: Visualization of extrusion and voids induced in copper-filled through-silicon vias (TSVs) at various temperatures using X-ray microscopy", Journal of Microelectronic Engineering, Vol. 92, pp. 24-28, 2012

[49] E. J. Marinissen, "Challenges in testing TSV-based 3D stacked ICs: Test Flows, Test Contents, and Test Aaccess", Prof. IEEE Asia Pacific Conference on Circuits and Systems, pp. 544-547, 2010

[50] C. W. Chou, J. F. Li, J. J. Chen, D. M. Kwai, Y. F. Chou and C. W. Wu, "A Test Integration Methodology for 3D Integrated Circuits", Proc. 19th IEEE Asian Test Symp., pp.377-382, 2010

[51] B. Noia, K. Chakrabarty and E. J. Marinissen, "Optimization Methods for

Post-Bond Die-Internal/External Testing in 3D Stacked ICs", Proc. IEEE International Test Conf., pp.1-9, 2010

[52] M. Gulbins, F. Hopsch, P. Schneider, B. Straube and W. Vermeiren, "Developing Digital Test Sequences for Through-Silicon Vias within 3D Structures", Proc. IEEE International 3D Systems Integration Conf., pp.1-6, 2010

[53] Y. J. Huang, J. F. Li, J. J. Chen, D. M. Kwai, Y. F. Chou and C. W. Wu, "A Built-In Self-Test Scheme for the Post-Bond Test of TSVs in 3D ICs", Proc. 29th IEEE VLSI Test Symp., pp.20-25, 2011

[54] K. Chakurabarty, M. Agrawal, S. Deutsch, B. Noia, R. Wang and F. Ye, "Test and Design-for-Testability Solutions for 3D Integrated Circuits", IPSJ Trans. on System LSI Design Methodology, Vol. 7, pp. 56-73, 2014

[55] C. C. Chi, E. J. Marinissen, S. Kumar Goel and C. W. Wu, "Post-Bond Testing of 2.5D-SICs and 3D-SICs Containing a Passive Silicon Interposer Base", Proc. IEEE International Test Conference, pp. 1-10, 2011

[56] Fara Ashikin, Masaki Hashizume, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, Zvi Roth, "A Design for Testability of Open Defects at Interconnects in 3D Stacked ICs", Journal of IEICE Transactions on Information and Systems, Vol. E101-D, No. 8, pp. 2053-2063, 2018

[57] Masaki Hashizume, Shoichi Umezu, Yuki Ikiri, Fara Ashikin Binti Ali, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, "Electrical Interconnect Test Method of 3D ICs without Boundary Scan Flip Flops", Proc. of IEEE CPMT Symposium Japan, pp. 136-139, 2015

[58] Fara Ashikin Binti Ali, Masaki Hashizume, Yuki Ikiri, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, "Testability of Resistive Open Defects by Electrical Interconnect Test of 3D ICs without Boundary Scan Flip Flops", Proc. of IEEE CPMT Symposium Japan, pp. 137-138, 2016

[59] Fara Ashikin Binti Ali, Yuki Ikiri, Masaki Hashizume, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, "Capacitive Open Defect Detection by Electrical Interconnect Test of 3D ICs without Boundary Scan Flip Flops", Proc. of 17th IEEE Workshop on RTL and High Level Testing, pp. 1.2.1-1.2.6, 2016

[60] F. Laermer, A. Schilp, "Method of anisotropically etching silicon", US patent 5,501,893, 1992

[61] B. Noia, K. Chakrabarty, "Pre-bond probing of TSVs in 3D stacked ICs", Proc. of IEEE International Test Conference, pp. 1-10, 2011

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List of Publications

Main Paper

1. Fara Ashikin, Masaki Hashizume, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, Zvi Roth, “A Design for Testability of Open Defects at Interconnects in 3D Stacked ICs”, IEICE Transactions on Information and Systems, Vol. E101-D, No. 8, pp. 2053-2063, August, 2018.

Sub Paper

1. Masaki Hashizume, Shoichi Umezu, Yuki Ikiri, Fara Ashikin Binti Ali, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, “Electrical Interconnect Test Method of 3D ICs without Boundary Scan Flip Flops”, Proc. of IEEE CPMT Symposium Japan, pp. 136-139, November, 2015.
2. Fara Ashikin Binti Ali, Masaki Hashizume, Yuki Ikiri, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, “Testability of Resistive Open Defects by Electrical Interconnect Test of 3D ICs without Boundary Scan Flip Flops”, Proc. of IEEE CPMT Symposium Japan, pp. 137-138, November, 2016.
3. Fara Ashikin Binti Ali, Yuki Ikiri, Masaki Hashizume, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, “Capacitive Open Defect Detection by Electrical Interconnect Test of 3D ICs without Boundary Scan Flip Flops”, Proc. of the 17th IEEE Workshop on RTL and High Level Testing, pp. 1.2.1-1.2.6, November, 2016.

Conference Paper

1. Akihiro Odoriba, Shoichi Umezu, Masaki Hashizume, Hiroyuki Yotsuyanagi, Ali Fara Ashikin Binti and Shyue-Kung Lu, “A Testable Design for Electrical Interconnect Tests of 3D ICs”, Proc. of International Conference on Electronics Packaging and iMAPS All Asia Conference, pp. 718-722, April, 2015.
2. Fara Ashikin Binti Ali, Akihiro Odoriba, Masaki Hashizume, Shoichi Umezu, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, “Electrical Tests of Capacitive Open

Defects at BGA ICs in Assembled PCB ”, Proc. of International Forum on Advanced Technologies, pp. 229-231, March, 2016.

3. Masaki Hashizume, Yuki Ikiri, Shoichi Umezu, Fara Ashikin Binti Ali, Hiroyuki Yotsuyanagi and Shyue-Kung Lu, “ Feasibility of Electrical Test for Open Defects at Address Bus in 3D Memory IC ”, Proc. of International Forum on Advanced Technologies, pp. 51-53, March, 2016.
4. Fara Ashikin Binti Ali, Shoichi Umezu, Yuki Ikiri, Hiroyuki Yotsuyanagi, Masaki Hashizume, Shyue-Kung Lu, “ Electrical Interconnect Test Method of Assembled PCBs without Boundary Scan Flip Flops ”, 第 30 回エレクトロニクス実装学会春季講演大会, pp. 195-197, March, 2016.
5. Fara Ashikin Binti Ali, Akihiro Odoriba, Masaki Hashizume, Hiroyuki Yotsuyanagi and Shyue-Kung Lu, “ Electrical Tests for Capacitive Open Defects in Assembled PCBs ”, Proc. of International Design and Concurrent Engineering Conference, September, 2016.
6. Fara Ashikin Ali, Akihiro Odoriba, Masaki Hashizume, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, “ Electrical Tests for Capacitive Open Defects in Assembled PCBs”, Journal of Telecommunication, Electronic and Computer Engineering, Vol. 9, No. 3-2, pp. 49-52, October, 2017.
7. Masashi Okamoto, Akihiro Odoriba, Fara Ashikin Binti Ali, Hiroyuki Yotsuyanagi, Masaki Hashizume and Shyue-Kung Lu, “ Feasibility of Capacitive Open Defect Detection with a Built-in Electrical Test Circuit Made of Diodes and nMOS Switches ”, Journal of Shikoku-Section Joint Convention of the Institutes of Electrical and Related Engineers, pp. 84, September, 2016.
8. Fara Ashikin Binti Ali, Masaki Hashizume, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, “ Test Circuit Design of Electrical Interconnect Test without Boundary Scan Flip Flops in 3D IC”, 4th International Forum on Advanced Technologies, P1-12, March, 2018.