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論　文　内　容　要　旨

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学位論文題目	Research on Interface State and Reliability of 4H-SiC MOSFETs with Thermal Gate Oxide （4H炭化ケイ素MOSFETゲート酸化膜の界面準位及び信頼性に関する研究）		

内容要旨

Silicon carbide (SiC) is a kind of IV–IV compound material with a wide bandgap and high critical (breakdown) electric field strength. The strong chemical bonding between Si and C atoms gives this material high hardness, chemical inertness, and high thermal conductivity. The ability of SiC to form silicon dioxide (SiO_2) as a native oxide is another important advantage for device fabrication. As a result of these properties, SiC has been developed as power metal–oxide–semiconductor field-effect transistors (MOSFETs) for high-power and high temperature electronics.

In a Si power MOSFET, the resistance of the drift layer cannot be neglected, but in a SiC power MOSFET, the drift layer resistance is nearly 100 times lower than that of a Si power MOSFET with the same blocking voltage, such as 1200 V. However, the channel resistance and the drift layer resistance are dominant factors in a SiC MOSFET when the blocking voltage is increased to 2–3 kV. When the blocking voltage is above 3 kV, the drift layer resistance of the SiC MOSFET becomes dominated, compared with that of a 600–1200 V Si power MOSFET. In addition, SiO_2 films can be directly grown on SiC substrates by conventional thermal oxidation, which is one of the advantages of SiC over other wide-gap semiconductors in device fabrication. Thermal oxidation of SiC has been believed to induce considerable interface defects at the SiO_2/SiC and near-interface traps. The interface defects not only reduce the channel mobility of SiC MOSFETs but also decrease the performance reliability.

According to the oxidation mechanism, it has been found that the oxidation reaction energy at the interface of SiO_2/SiC (3.12 eV) is larger than that at the interface of SiO_2/Si (1.23 eV). It is widely accepted that the oxidation temperature affects the oxidation rate. With an increase of the temperature, the interface reaction rate significantly increases while the diffusion rate decreases. For this problem, we confirmed that the optimal D_{it} was obtained for the sample oxidized at 1450°C in the energy range 0.2–0.6 eV below the conduction band edge of SiC. However, there was a trade-off between D_{it} and reliability, the sample oxidized at 1250°C showed the most reliable character of those tested. To ease the tradeoff between interface state and reliability, Argon (Ar) and Nitric oxide (NO) post oxidation anneal (POA) was research. During the further results, we found that the reduction of D_{it} is mainly attributing to NO annealing and higher temperature. However, due to the introduction of N positive charge, the flat band voltage of the SiC-MOS capacitor devices drifts in the negative direction, which will form normally on SiC-MOSFETs. On the other hands, even though Ar annealing can keep the flat band voltage comparing with the as grown one, but it is proof to weekly improve the quality of oxide layer near the SiO_2/SiC interface and enhance the effect of NO annealing.

We also revealed that the interface state density near the conductance band reduces significantly when the annealing temperature reaches to 1300°C or the annealing time extends to 120 min by further experiments. It is suggested that the interface state density reduces when the POA temperature was elevated or the POA time was extended. We also worked that the effects of NO annealing temperature and time on the reliability of 4H-SiC MOS gate oxide. And from the results of field-to-breakdown (E_{BD}) and charge-to-breakdown (Q_{BD}), find it is effectively improving the insulation properties and reliability of gate oxide by high temperature NO annealing.

Related studies have shown that controlling the macro stress of SiC materials and the local stress generated by defects is benefit on improving the interface

characteristics of SiC devices, indicating that the mechanism of the thermal oxide reliability of SiC MOS devices revealed by stress research is necessary. Recently, research already has gradually focused on the process to the SiC material itself. It is expected to improve the interface problems of SiC MOS devices. In this paper, by commercial silicon carbide epitaxial material, the defects on the interface state and reliability of the gate oxide film are investigated. The effect of grinding-induced stress on interface state density of SiC/SiO_2 was investigated and also calculated by first-principle calculations, and the energy levels (E_0) of the samples related to the lattice constants of the SiC crystal, indicating that stress mainly affected the SiO_2/SiC interface. Furthermore, we studied the excessive compressive/tensile curvature, induced by stress/strain, decreased reliability of SiO_2 films, expressed by E_{BD} and Q_{BD} during dry thermal oxidation processes. We suggest that a "stress free" oxide film might be the best choice for SiC-MOSFET applications. These results will be useful for industrial applications of SiC and SiC-based devices and practical epitaxy wafer selection.